EE4390 Microprocessors

Lessons 27, 28
Serial Peripheral Interface
Serial Peripheral Interface

- Synchronous serial communication system
- Transmitter and receiver share common clock
- Clock signal provided by Master configured device and fed to Slave configured devices
- SPI data link is considerably faster than the SCI at the expense of an additional line
- SPI operates as a geographically distributed shift register
Serial Peripheral Interface

- SPI acts as 16-bit distributed shift register
- Shares common clock (SCK) provided by Master configured device
- Signals
  - SCK
  - MOSI
  - MISO
  - Slave Select (SS)
Serial Peripheral Interface
Serial Peripheral Interface
SPI Activities

Initialize SPI
- configure Port S and DDRS for SPI operation
- set serial clock rate in SPI Baud Rate Register (SP0ER)
- configure SPI Control Registers (SP0CR1,2) with desired SPI parameters
- clear the SPIF flag
- enable the SPI using SPE bit in SP0CR1
- return from subroutine (RTS)

Transmit Character
- Assert $S$ line to start transmission
- write to SPI Data Register (SP0DR)
- poll SPI Status Register (SP0SR)
- De-assert $SS$ line to stop transmission
- return from subroutine (RTS)

Receive Character
- poll SPI Status Register (SP0SR)
- SPIF = 1
- yes
- no
- SPIF = 1
- yes
- return from subroutine (RTS)
- SPIF = 1
- no
- return from subroutine (RTS)
- SPIF = 1
- yes
SPI Applications

• Extend features of 68HC12
  – additional memory components
  – Additional ports
  – Real-time clock
  – Phase-locked loop
  – FM transmitter/receiver
  – high-resolution analog-to-digital
  – LCD display
  – multi-channel digital-to-analog converter
SPI Applications
- multi-channel digital-to-analog converter -

![Diagram of multi-channel digital-to-analog converter](image)
SPI Applications
- multi-channel digital-to-analog converter -

S3 -- ENE
MCSI -- Din
MOSI
SCK -- CLK

CPU12
S3
SCK
MOSI

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