EE4390 Microprocessors

Lessons 2, 3
68HC12 Hardware Overview, Subsystems, and memory System
Overview

- 68HC12 hardware overview
- Subsystems
- Memory System
68HC12 Hardware Overview

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68HC12 Hardware Overview (cont)

• Timing System
• Memory System
• Interrupt and Reset System
• Serial Communication System
• Port System
• Data Conversion System
68HC12 Hardware Overview (cont)

• Low power consumption - CMOS technology, “A4” draws 25 mA @ 2 MHz
• 16-bit data path (we will use in 8-bit mode)
• A4 memory:
  – 1024-byte RAM
  – 4 K-byte EEPROM
• 8-channel, 16-bit timer, configure each channel separately as input or output
• 16-bit pulse accumulator
68HC12 Hardware Overview (cont)

- Real-time interrupt capability - accomplish operations on recurring basis - reminder

- Serial communications:
  - Serial Communication Interface (SCI)
    - asynchronous, 2 channels
  - Serial Peripheral Interface (SPI)
    - synchronous

- 8-channel, 8-bit analog-to-digital converter
68HC12 Hardware Overview (cont)

- Modes of Operation
  - Normal
  - Special
- Configure using BKGD, MODB, and MODA hardware pins
- Normal modes:
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode - 16-bit data bus
  - Normal Expanded Narrow Mode - 8-bit data bus
68HC12 Hardware Overview (cont)

• “A4” available in 122-pin TQFP - Fig 5.6, pg. 176
  – voltage supply or reference pins
  – port pins
  – miscellaneous pins - external signals
68HC12 Subsystems
Register Block

• Register Block
  – 512-byte memory map collection of registers
  – Registers used to configure 68HC12 for specific tasks
    • turn subsystems “on” and “off”, configure operation
    • default register settings

EX] ATDCTL2 = $0062 ;register offset from base
ATD_INI = $80 ;register mask or value

LDAA #ATD_INI
STAA ATDCTL2

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68HC12 Subsystems
Port System

• Port System
  – used to exchange data and control signals with outside environment
  – Port is either an input register, output register, or configurable I/O register
  – Multiple ports
    • A - H, J general purpose I/O ports in single chip mode, have other functions in expanded mode
    • S: serial communication, T: timer system, AD: analog-to-digital
68HC12 Subsystems
Port System - (cont)

• Port related registers:
  – Data Direction Register (DDRx): configures Port as input/output (1: output, 0: input)
  – Pull Up Control Register (PUCR): provides built-in pull-up resistor for interface applications
  – Reduced Drive of I/O Lines Register (RDRIV): reduces current drive capability of pin
  – Port E Assignment Register (PEAR):
    • provides alternate bus functions in expanded mode
    • signals used in memory expansion applications
68HC12 Subsystems
The Timing System - Standard Timer Module (TIM)

• TIM contains 16-bit programmable counter
• Provides following precision timer functions:
  – Input capture: measure the characteristics of incoming signals such as frequency, period, duty cycle, pulse length
  – Output compare: generate precision output signals such as periodic digital waveforms, pulses, etc.
  – Pulse accumulator: count external events
  – Pulse Width Modulated (PWM) signal generation
    • PWM not available in “A4” variant
68HC12 Subsystems
The Memory System
68HC12 Subsystems
The Memory System (cont)

• Data bus width = memory width = M
• memory locations = $2^{\text{addr lines}} = 2^n$
• Memory expressed as length x width
  – $2^n$ x M bits
• 68HC12
  – 16-bit address bus
    • 1st address: %0000_0000_0000_0000 = $0000$
    • last address: %1111_1111_1111_1111 = $FFFF$
    • $2^{16}$ locations = 65, 536 locations ~ 64K
  – 16-bit data bus (we will use 8-bit configuration)
68HC12 Subsystems
The Memory System (cont)

• Memory Technologies:
  – RAM: Random Access Memory
    • volatile: no power, no memory
    • read/write
    • faster access time than ROM
    • temporary data storage during program execution
    • program storage during code development
  – ROM: Read Only Memory
    • nonvolatile
    • read
    • stores instructions and constants
    • byte-erasable EEPROMs, flash EEPROMs
    • program storage in final code version
68HC12 Subsystems
The Memory System (cont)

• Memory Map tracks memory usage in uP

Figure 5.8 A4 memory map. (Figure used with permission of Motorola, Incorporated.)

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68HC12 Subsystems
Interrupts

- Break in normal program execution
- Usually higher priority event
- In response to interrupt, 68HC12:
  - finishes current instruction
  - stores key register values
  - performs an Interrupt Service Routine (ISR) specific for that interrupt
# 68HC12 Subsystems

## Interrupts (cont)

<table>
<thead>
<tr>
<th>Vector Address</th>
<th>Interrupt Source</th>
<th>CCR Mask</th>
<th>Local Enable</th>
<th>HPRIO Value to Elevate</th>
</tr>
</thead>
<tbody>
<tr>
<td>$FFFFE, $FFFD</td>
<td>Reset</td>
<td>none</td>
<td>none</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFC, $FFFD</td>
<td>COP Clock Monitor Fail Reset</td>
<td>none</td>
<td>CME, FCME</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFFA, $FFFB</td>
<td>COP Failure Reset</td>
<td>none</td>
<td>cop rate selected</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFE, $FFFF</td>
<td>Unimplemented Instruction Trap</td>
<td>none</td>
<td>none</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFF, $FFFE</td>
<td>SWI</td>
<td>none</td>
<td>none</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFF4, $FFFF5</td>
<td>XIRQ</td>
<td>x bit</td>
<td>none</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFF2, $FFFF3</td>
<td>IRQ or Key Wake Up D</td>
<td>1 bit</td>
<td>IRQEN, KWIED(7:0)</td>
<td>$F2</td>
</tr>
<tr>
<td>$FFFF0, $FFFF1</td>
<td>Real Time Interrupt</td>
<td>1 bit</td>
<td>RTIE</td>
<td>$F0</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 0</td>
<td>1 bit</td>
<td>TC0</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 1</td>
<td>1 bit</td>
<td>TC1</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 2</td>
<td>1 bit</td>
<td>TC2</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 3</td>
<td>1 bit</td>
<td>TC3</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 4</td>
<td>1 bit</td>
<td>TC4</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 5</td>
<td>1 bit</td>
<td>TC5</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 6</td>
<td>1 bit</td>
<td>TC6</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFEA, $FFFE1</td>
<td>Timer Channel 7</td>
<td>1 bit</td>
<td>TC7</td>
<td>$EE</td>
</tr>
<tr>
<td>$FFFD, $FFFD</td>
<td>Timer Overflow</td>
<td>1 bit</td>
<td>TOI</td>
<td>$DE</td>
</tr>
<tr>
<td>$FFDC, $FFDD</td>
<td>Pulse Accumulator Overflow</td>
<td>1 bit</td>
<td>PAOV1</td>
<td>$DC</td>
</tr>
<tr>
<td>$FFDA, $FFDB</td>
<td>Pulse Accumulator Input Edge</td>
<td>1 bit</td>
<td>PAI</td>
<td>$DA</td>
</tr>
<tr>
<td>$FFD8, $FFD9</td>
<td>SPI Serial Transfer Complete</td>
<td>1 bit</td>
<td>SPIOE</td>
<td>$D8</td>
</tr>
<tr>
<td>$FFD6, $FFD7</td>
<td>SCI 0</td>
<td>1 bit</td>
<td>TIE0,TIE0,</td>
<td>$D6</td>
</tr>
<tr>
<td>$FFD4, $FFD5</td>
<td>SCI 1</td>
<td>1 bit</td>
<td>TIE1,TIE1,</td>
<td>$D6</td>
</tr>
<tr>
<td>$FFD2, $FFD3</td>
<td>ATD</td>
<td>1 bit</td>
<td>ADIE</td>
<td>$D2</td>
</tr>
<tr>
<td>$FFD0, $FFD1</td>
<td>Key Wakeup J (stop wakeup)</td>
<td>1 bit</td>
<td>KWIEJ(7:0)</td>
<td>$D0</td>
</tr>
<tr>
<td>$FFC5, $FFCF</td>
<td>Key Wakeup H (stop wakeup)</td>
<td>1 bit</td>
<td>KWIEH(7:0)</td>
<td>$C6</td>
</tr>
<tr>
<td>$FF80–$FFCD</td>
<td>Reserved</td>
<td>1 bit</td>
<td>$B0–$CC</td>
<td>$B0–$CC</td>
</tr>
</tbody>
</table>

**Figure 5.9**  Interrupt vector map. (Figure used with permission of Motorola, Incorporated.)

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68HC12 Subsystems
Serial Communications - Multiple Serial Interface

- Serial Communication Interface (SCI)
  - asynchronous
  - two channels
  - single line
  - uses start and stop bit to frame each ASCII character

- Serial Peripheral Interface (SPI)
  - synchronous
  - one channel
  - shares clock between Master and Slave designated devices
  - requires additional clock line
  - much faster data transmission than SCI
68HC12 Subsystems
Analog-to-Digital Converter

• Analog world -- digital processor
• Converts analog sample to unsigned, weighted binary value
• 8-channel, 8-bit successive approximation converter

\[ V_{RH} \]
\[ V_{RL} \]
\[ $00 \] \quad \[ $FF \]
EX] Remote Weather Station
EX] Remote Weather Station (cont)

- Anemometer - wind velocity, pulse every time it completes revolution
- Barometer - barometric pressure, 0 V for 64 cm of Hg, 5 V for 81 cm of Hg
- Hygrometer - relative humidity, 0 V for 0%, 5 V for 100% relative humidity
- Rain gauge - 20 mV/cm precipitation
- thermocouple - temperature, 0 V for -50 degrees C, 5 V for +120 degrees C
- weather vane - wind direction 0 V North, 5V back to North