University of Wyoming
EE/COSC 2390 Digital Systems Design
Spring Semester, 2004
Course Syllabus (Section 01 — Hamann)

Session	Date		Topic	Reading	Hwk Due
1	1/21	W	Intro to Digital Design, Number Systems	Ch. 1 pp. 1–13	
2	1/23	F	Addition/Subtraction, Overflow	Ch. 1 pp. 13–16	Set #1 Assigned
3	1/26	M	More Arithmetic, Binary Codes	Ch. 1 pp. 16–24	
4	1/28	W	Registers, Binary Logic	Ch. 1 pp. 24–30	
5	1/30	F	Boolean Algebra and Functions	Ch. 2 pp. 33–44	Set #1 Due
6	2/2	M	Canonical and Standard Forms, Other Ops	Ch. 2 pp. 44–53	
7	2/4	W	Digital Logic Gates, Integrated Circuits	Ch. 2 pp. 53–61	
8	2/6	F	Gate Minimization, Karnaugh Maps	Ch. 3 pp. 64–79	Set #2 Due
9	2/9	M	More K-Maps, Don't Cares	Ch. 3 pp. 80–99	
10	2/11	W	Finish Minimization	Notes	
11	2/13	F	Intro to HDLs	Ch. 3, pp. 99–106	Set #3 Due
12	2/16	M	Combinational Logic Design, Bubbles	Ch. 4 pp. 111–118	
13	2/18	W	Arithmetic Operations and Logic	Ch. 4 pp. 119–134	
14	2/20	F	Decoders/Encoders, Muxes	Ch. 4 pp. 134–147	Set #4 Due
15	2/23	M	Finish Combinational Design Examples	Notes, Ch. 7 pp. 275–283	
16	2/25	W	Combinational HDL and Test Benches	Ch. 4 pp. 147–160	
17	2/27	F	Summary for Exam #1	Notes	Set #5 Due
18	3/1	M	**Exam #1**	Ch. 1–4	
19	3/3	W	More Combinational HDL	Notes	
20	3/5	F	Intro Synchronous Sequential Logic	Ch. 5 pp. 167–179	
21	3/8	M	Analysis of Clocked Sequential Circuits	Ch. 5 pp. 180–190	
22	3/10	W	HDL for Sequential Logic	Ch. 5 pp. 190–198	
23	3/12	F	More Sequential HDL	Notes	Set #6 Due
	3/15–3/19	M–F	*Spring Break*		
24	3/22	M	State Reduction and Assignment	Ch. 5 pp. 198–203	
25	3/24	W	Sequential Design Procedures	Ch. 5 pp. 203–211	
26	3/26	F	Registers and Applications	Ch. 6 pp. 217–227	Set #7 Due
27	3/29	M	Binary and BCD Ripple Counters	Ch. 6 pp. 227–232	
28	3/31	W	Synchronous Binary and BCD Counters	Ch. 6 pp. 232–239	
29	4/2	F	Other Counters and HDL	Ch. 6 pp. 239–249	Set #8 Due
30	4/5	M	Register Transfer Level Notation	Ch. 8 pp. 291–299	
31	4/7	W	Algorithmic State Machines	Ch. 8 pp. 299–310	Set #9 Due
	4/9	F	*Easter Break*		
32	4/12	M	Summary for Exam #2	Notes	
33	4/14	W	**Exam #2**	Ch. 4–6	
34	4/16	F	HDL for ASMs	Ch. 8 pp. 310–317	
35	4/19	M	More ASM Design Examples	Ch. 8 pp. 317–336	
36	4/21	W	More ASM Design Examples	Notes	
37	4/23	F	Asynchronous Sequential Logic Intro	Ch. 9 pp. 342–352	Set #10 Due
38	4/26	M	Latch Design Procedures	Ch. 9 pp. 352–366	
39	4/28	W	Reduction, Timing, Hazards	Ch. 9 pp. 367–384	
40	4/30	F	Asynchronous Examples	Ch. 9 pp. 384–390	Set #11 Due
41	5/3	M	Memory, Error Detection and Correction	Ch. 7 pp. 255–276	
42	5/5	W	PLAs, PALs, CPLDs, FPGAs	Ch. 7 pp. 276–287	
43	5/7	F	Summary for Exam #3	Notes	Set #12 Due
	5/10	M	**Final Exam 10:15 – 12:15** for MWF 10:00	Summary	

Note: This schedule is subject to change: official times will be announced in class. **Remember, a brief quiz will be given each week!**

EE/COSC 2390 Course Information and Policies

Instructor: Jerry C. Hamann
Rm. 5036 Engineering and Rm. 2070 Engineering
Office Phone 766-6321 (email: hamann@uwyo.edu)

Office Hours: `MWF 9:00 -- 9:50, MW 2:10 -- 3:00`

Text: *Digital Design,*
M. Morris Mano, 3rd Edition, Prentice-Hall, 2002.

Grading:

Hour Exams	40%
Final Exam	25%
Homework	10%
Quizzes	10%
Laboratory	12%
Lab Notebooks	3%
Total	100%

Prerequisites: Students should have completed MATH 2205 (Calculus II).

Course Description: Binary logic, digital logic gates, reduction of Boolean expressions, combinational logic design. MSI and LSI combinational logic ICs, flip-flops, synchronous and asynchronous sequential systems design, MSI and LSI sequential system ICs, and algorithmic state machines.

Quizzes/Exams: A brief quiz will be given in class each week. Examinations will be given on the days noted on the Course Syllabus, unless circumstances dictate a change which will be announced in class. It is not possible to make up a missed quiz or exam without a University Excused Absence.

Homework: Homework sets will be given on a near weekly basis, with due dates as shown on the Course Syllabus. **Assignments must be handed in at class time on the specified due date. No credit will be given for late assignments.** Please work neatly, showing all of your solution process and clearly indicating all answers by underlining them or drawing a box around them. **Solutions to the homework will be posted on the Digital Systems Design Web Site at** `http://wwweng.uwyo.edu/classes/sp2004/ee2390` **.** Typically just one problem from the set will be graded; students are responsible for verifying the solutions of the remainder.

Laboratory: Attendance at labs is required. You **MUST** attend the lab in which you are enrolled. Satisfactory completion of each and every lab exercise is required in order to pass the course. Refer to the EE/COSC 2390 Laboratory Policies handout for further details.

Suggestions: Some recommendations for study which you should consider are as follows...

Don't miss class. New material is covered each lecture. If you miss class, you are responsible for covering the missed material. Repeat lectures will not be given during office hours.

Read in advance. The reading assignments are detailed on the Syllabus. Please note that the argument "but the book is difficult to read" receives very little respect in any forum.

Start homework early. Give yourself some time to consider the problems and determine whether or not you need instructor assistance. Last-minute questions are not a good idea.

Don't ignore the homework, lab and quizzes. They comprise 35% of your grade. **If you do not satisfactorally complete each and every lab exercise, you will fail the course, as specified in the policies and regulations of the Department of Electrical and Computer Engineering.**

Ask questions. This includes during class, during labs and during office hours.

Policies Regarding Assignments: Students are encouraged to discuss course topics and assignments with one another. However, **the homework solutions, prelabs, quizzes and exams turned in by each student must consist of that individual's own work** as noted in the Department of Electrical and Computer Engineering Course Policies (available in the Department Office) and the University of Wyoming Academic Policies and Procedures.