EE4390 Microprocessors

Lessons 2, 3

68HC12 Hardware Overview, Subsystems, and memory System

Overview

- 68HC12 hardware overview
- Subsystems
- Memory System

68HC12 Hardware Overview

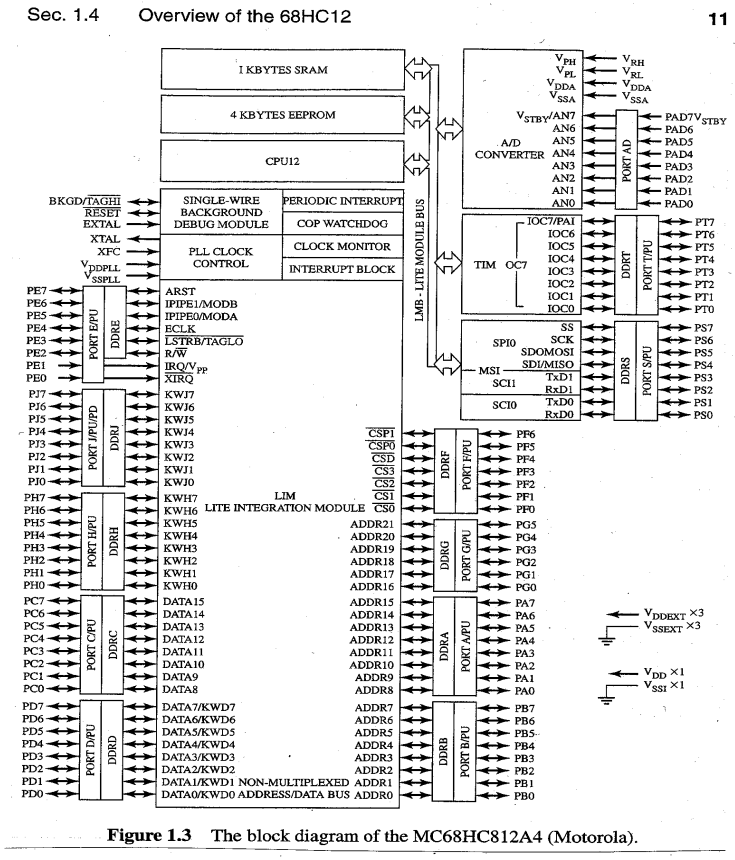

Figure 1.3 The block diagram of the MC68HC812A4 (Motorola).

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68HC12 Hardware Overview (cont)

- Timing System
- Memory System
- Interrupt and Reset System
- Serial Communication System
- Port System
- Data Conversion System

68HC12 Hardware Overview (cont)

- Low power consumption - CMOS technology, “A4” draws 25 mA @ 2 MHz
- 16-bit data path (we will use in 8-bit mode)
- A4 memory:
  - 1024-byte RAM
  - 4 K-byte EEPROM
- 8-channel, 16-bit timer, configure each channel separately as input or output
- 16-bit pulse accumulator

68HC12 Hardware Overview (cont)

- Real-time interrupt capability - accomplish operations on recurring basis - reminder
- Serial communications:
  - Serial Communication Interface (SCI)
    - asynchronous, 2 channels
  - Serial Peripheral Interface (SPI)
    - synchronous
- 8-channel, 8-bit analog-to-digital converter

68HC12 Hardware Overview (cont)

- Modes of Operation
  - Normal
  - Special
- Configure using BKGD, MODB, and MODA hardware pins
- Normal modes:
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode - 16-bit data bus
  - Normal Expanded Narrow Mode - 8-bit data bus

68HC12 Hardware Overview (cont)

- “A4” available in 122-pin TQFP - Fig 5.6, pg. 176
  - voltage supply or reference pins
  - port pins
  - miscellaneous pins - external signals

68HC12 Subsystems
Register Block

- Register Block
  - 512-byte memory map collection of registers
  - Registers used to configure 68HC12 for specific tasks
    - turn subsystems “on” and “off”, configure operation
    - default register settings

```
EX]     ATDCTL2         =   $0062 ;register offset from base
        ATD_INI         =   $80     ;register mask or value

        LDAA    #ATD_INI
        STAA    ATDCTL2
```

68HC12 Subsystems
Port System

- Port System
  - used to exchange data and control signals with outside environment
  - Port is either an input register, output register, or configurable I/O register
  - Multiple ports
    - A - H, J general purpose I/O ports in single chip mode, have other functions in expanded mode
    - S: serial communication, T: timer system,

      AD: analog-to-digital

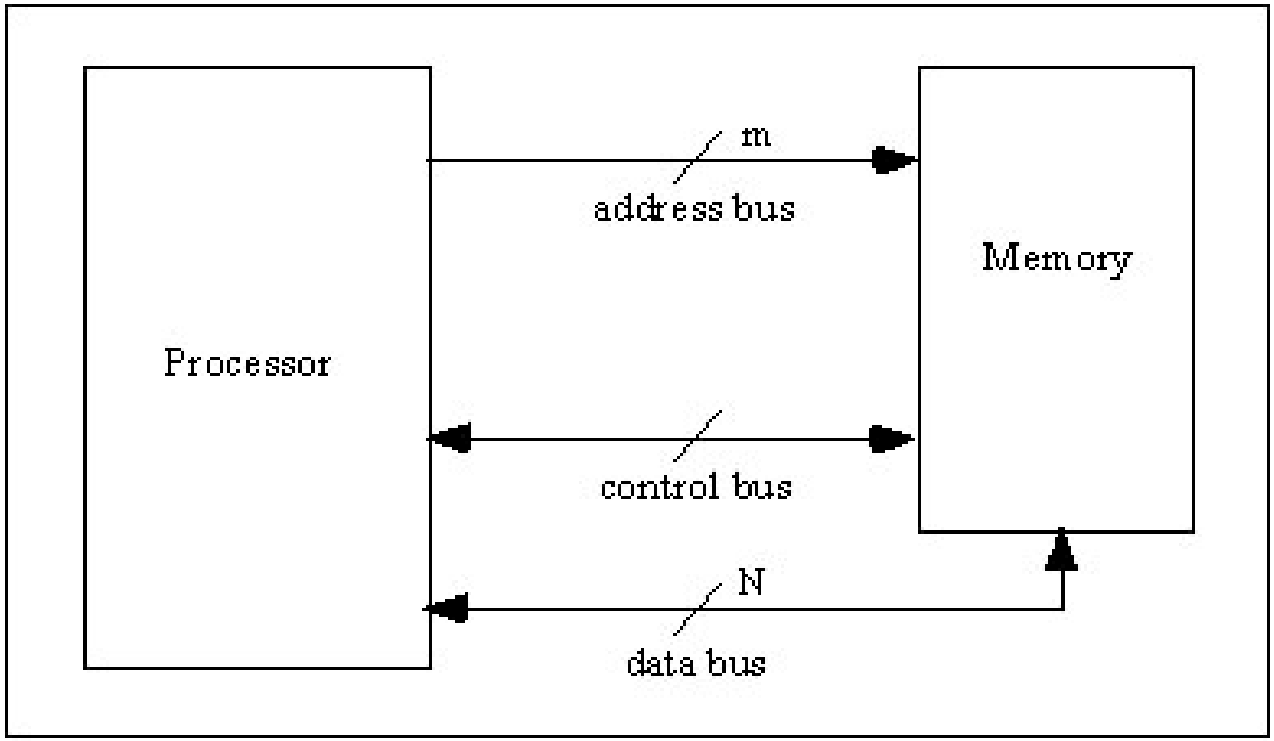
68HC12 Subsystems
Port System - (cont)

- Port related registers:
  - Data Direction Register (DDRx): configures Port as input/output (1: output, 0: input)
  - Pull Up Control Register (PUCR): provides built-in pull-up resistor for interface applications
  - Reduced Drive of I/O Lines Register (RDRIV): reduces current drive capability of pin
  - Port E Assignment Register (PEAR):
    - provides alternate bus functions in expanded mode
    - signals used in memory expansion applications

68HC12 Subsystems
The Timing System - Standard Timer Module (TIM)

- TIM contains 16-bit programmable counter
- Provides following precision timer functions:
  - Input capture: measure the characteristics of incoming signals such as frequency, period, duty cycle, pulse length
  - Output compare: generate precision output signals such as periodic digital waveforms, pulses, etc.
  - Pulse accumulator: count external events
  - Pulse Width Modulated (PWM) signal generation
    - PWM not available in “A4” variant

68HC12 Subsystems
The Memory System



68HC12 Subsystems
The Memory System (cont)

- Data bus width = memory width = M
- memory locations = $2^{\text{addr lines}} = 2^n$
- Memory expressed as length x width
  - 2^n x M bits
- 68HC12
  - 16-bit address bus
    - 1st address: %0000_0000_0000_0000 = $0000
    - last address: %1111_1111_1111_1111 = $FFFF
    - 2^{16} locations = 65, 536 locations ~ 64K
  - 16-bit data bus (we will use 8-bit configuration)

68HC12 Subsystems
The Memory System (cont)

- Memory Technologies:
  - RAM: Random Access Memory
    - volatile: no power, no memory
    - read/write
    - faster access time than ROM
    - temporary data storage during program execution
    - program storage during code development
  - ROM: Read Only Memory
    - nonvolatile
    - read
    - stores instructions and constants
    - byte-erasable EEPROMs, flash EEPROMs
    - program storage in final code version

68HC12 Subsystems
The Memory System (cont)

- Memory Map tracks memory usage in uP

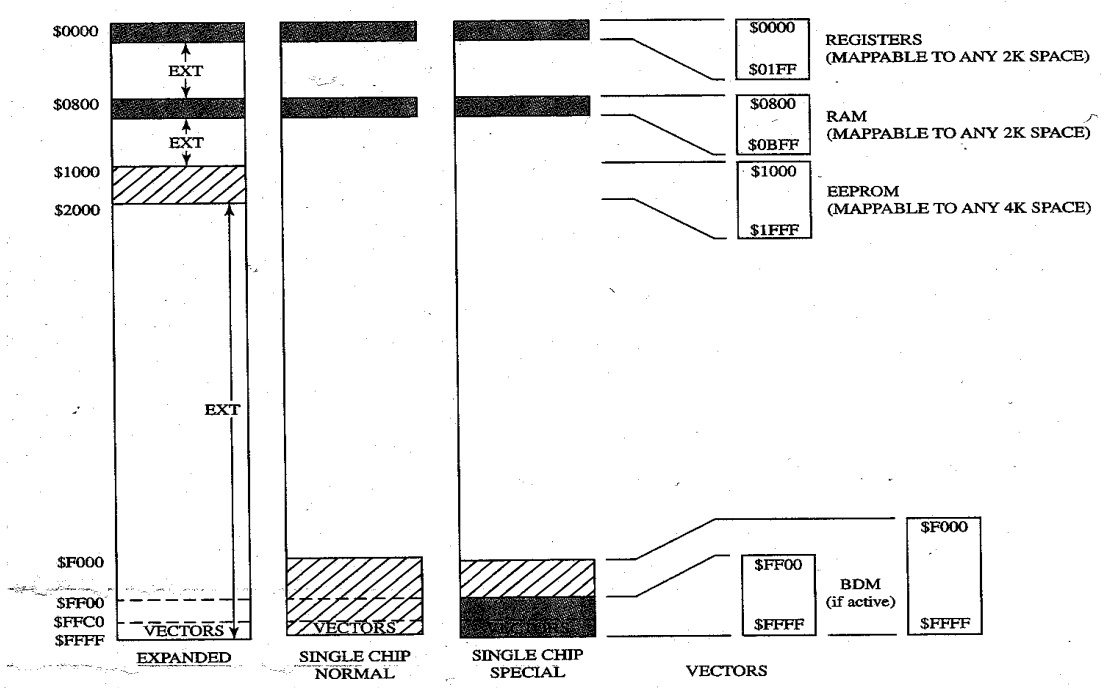
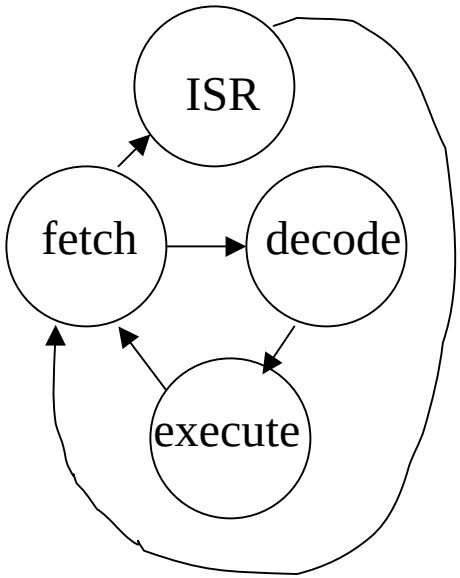


Figure 5.8 A4 memory map. (Figure used with permission of Motorola, Incorporated.)

68HC12 Subsystems
Interrupts



- Break in normal program execution
- Usually higher priority event
- In response to interrupt, 68HC12:
  - finishes current instruction
  - stores key register values
  - performs an Interrupt Service Routine (ISR) specific for that interrupt

68HC12 Subsystems
Interrupts (cont)

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	Reset	none	none	–
$FFFC, $FFFD	COP Clock Monitor Fail Reset	none	CME, FCME	–
$FFFA, $FFFB	COP Failure Reset	none	cop rate selected	–
$FFF8, $FFF9	Unimplemented Instruction Trap	none	none	–
$FFF6, $FFF7	SWI	none	none	–
$FFF4, $FFF5	XIRQ	x bit	none	–
$FFF2, $FFF3	IRQ or Key Wake Up D	1 bit	IRQEN, KWIED(7:0)	$F2
$FFF0, $FFF1	Real Time Interrupt	1 bit	RTIE	$F0
$FFEE, $FFEF	Timer Channel 0	1 bit	TC0	$EE
$FFEC, $FFED	Timer Channel 1	1 bit	TC1	$EC
$FFEA, $FFEB	Timer Channel 2	1 bit	TC2	$EA
$FFE8, $FFE9	Timer Channel 3	1 bit	TC3	$E8
$FFF6, $FFE7	Timer Channel 4	1 bit	TC4	$E6
$FFF4, $FFE5	Timer Channel 5	1 bit	TC5	$E4
$FFF2, $FFE3	Timer Channel 6	1 bit	TC6	$E2
$FFE0, $FFE1	Timer Channel 7	1 bit	TC7	$E0
$FFDE, $FFDF	Timer Overflow	1 bit	TOI	$DE
$FFDC, $FFDD	Pulse Accumulator Overflow	1 bit	PAOVI	$DC
$FFDA, $FFDB	Pulse Accumulator Input Edge	1 bit	PAII	$DA
$FFD8, $FFD9	SPI Serial Transfer Complete	1 bit	SPI0E	$D8
$FFD6, $FFD7	SCI 0	1 bit	TIE0,TCIE0, RIE0,ILIE0	$D6
$FFD4, $FFD5	SCI 1	1 bit	TIE1,TCIE1, RIE1,ILIE1	$D4
$FFD2, $FFD3	ATD	1 bit	ADIE	$D2
$FFD0, $FFD1	Key Wakeup J (stop wakeup)	1 bit	KWIEJ(7:0)	$D0
$FFCE, $FFCF	Key Wakeup H (stop wakeup)	1 bit	KWIEH(7:0)	$CE
$FF80–$FFCD	Reserved	1 bit		$B0–$CC

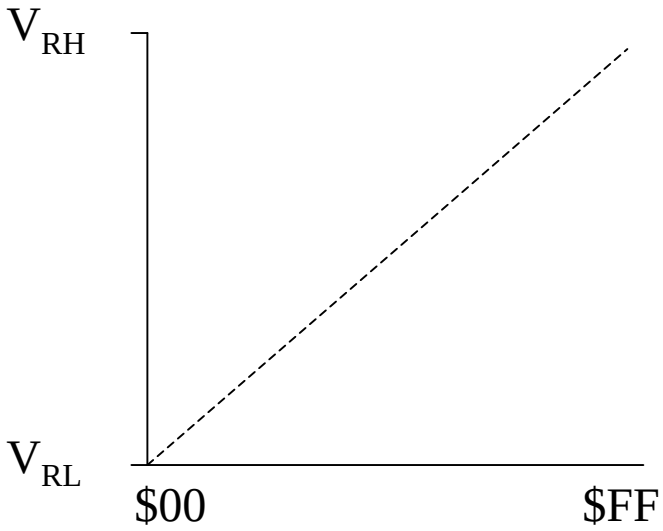
Figure 5.9 Interrupt vector map. (Figure used with permission of Motorola, Incorporated.)

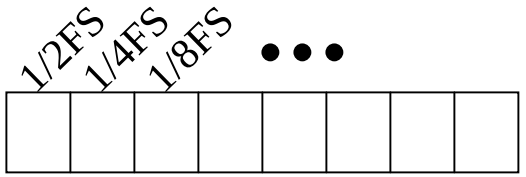
68HC12 Subsystems
Serial Communications - Multiple Serial Interface

- Serial Communication Interface (SCI)
  - asynchronous
  - two channels
  - single line
  - uses start and stop bit to frame each ASCII character
- Serial Peripheral Interface (SPI)
  - synchronous
  - one channel
  - shares clock between Master and Slave designated devices
  - requires additional clock line
  - much faster data transmission than SCI

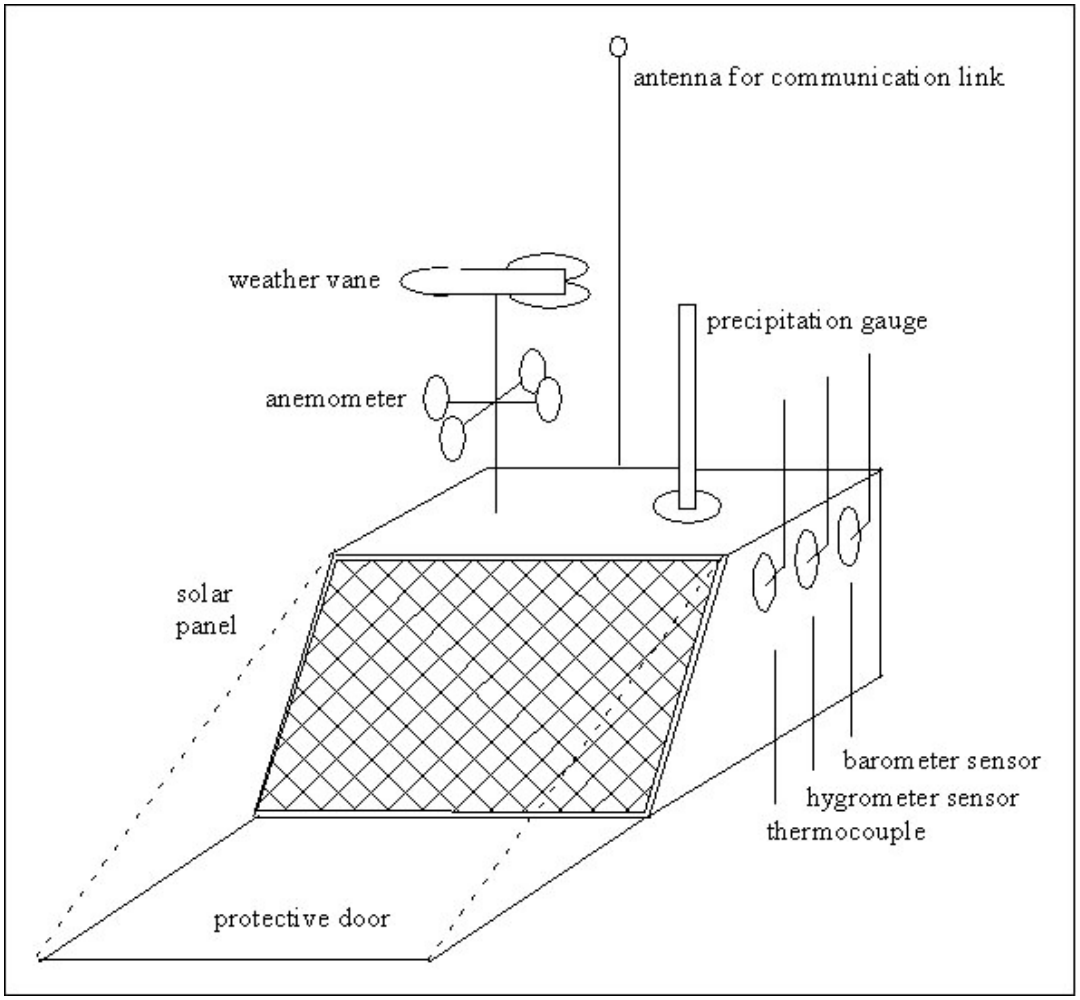
68HC12 Subsystems
Analog-to-Digital Converter

- Analog world -- digital processor
- Converts analog sample to unsigned, weighted binary value
- 8-channel, 8-bit successive approximation converter





EX] Remote Weather Station



EX] Remote Weather Station (cont)

- Anemometer - wind velocity, pulse every time it completes revolution
- Barometer - barometric pressure, 0 V for 64 cm of Hg, 5 V for 81 cm of Hg
- Hygrometer - relative humidity, 0 V for 0%, 5 V for 100% relative humidity
- Rain gauge - 20 mV/cm precipitation
- thermocouple - temperature, 0 V for - 50 degrees C, 5 V for +120 degrees C
- weather vane - wind direction 0 V North, 5V back to North