EE4390
Microprocessors

Lessons 9, 10
Serial Communications Interface

Overview

- Fundamentals and Terminology
- Signals
- Multiple Serial Interface
- Serial Communications Interface (SCI)
  - Transmitter
  - Receiver
  - Registers
- SCI Programming
- RS-232 interface

Fundamentals and Terminology

- Serial communication link - single line connection, data sent one bit at a time
- clock - establishes rate of data transfer
- bit rate - bits per second
- bit cell - time to transmit a single bit
- BAUD rate - bits per second
- NRZ line code - transmit value for entire bit cell

Fundamentals and Terminology (cont)

- ASCII - American Standard Code for Information Interchange

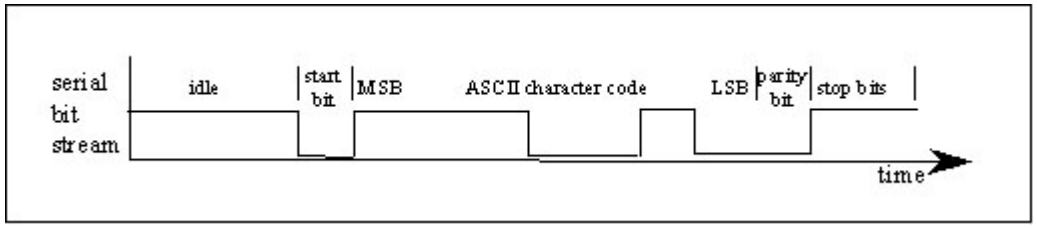
ASCII CHARACTER SET (7-Bit Code)

LS Dig. \ MS Dig.	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

ASCII CHART

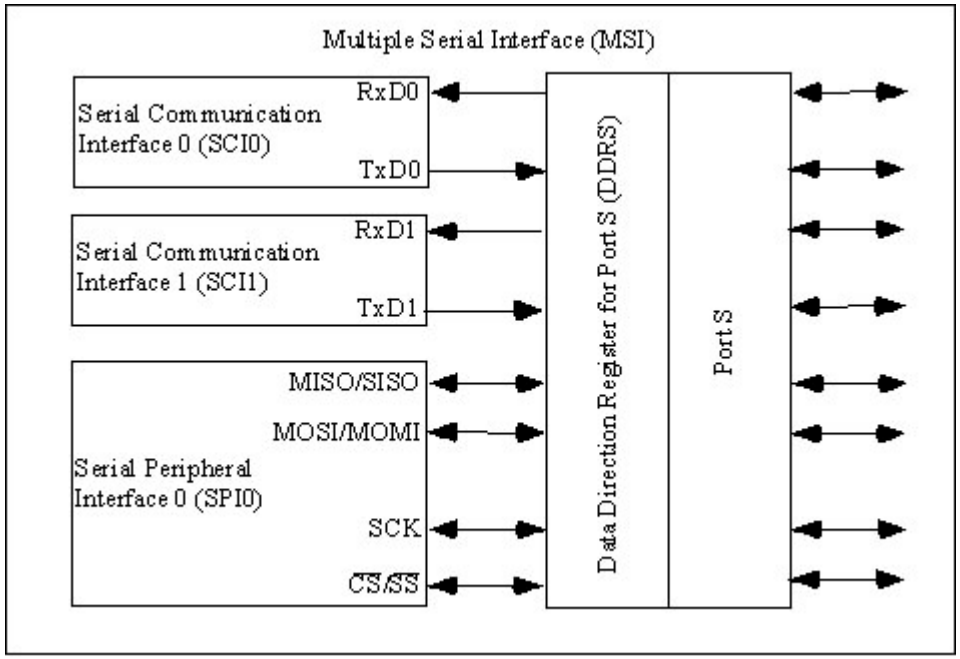
Fundamentals and Terminology (cont)

- Parity bit - used to detect a single error
  - odd parity: odd number of ones in character
  - even parity: even number of ones in character
- Simplex: transmit or receive data, not simultaneously



Multiple Serial Interface

- Two SCI channels and one SPI channel



Serial Communications Interface (SCI) Transmitter

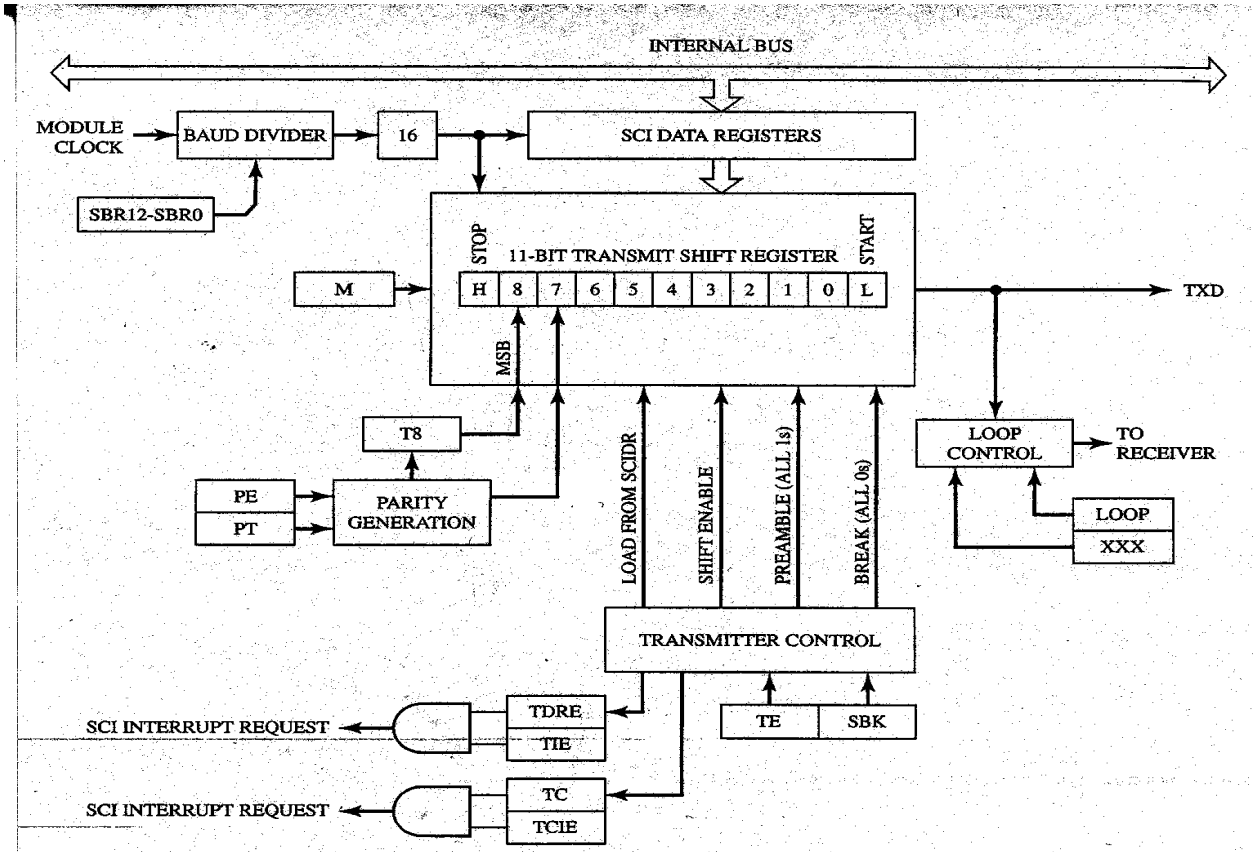


Figure 10.8 The SCI transmitter. (Figure used with permission of Motorola, Incorporated.)

Serial Communications Interface (SCI) Receiver

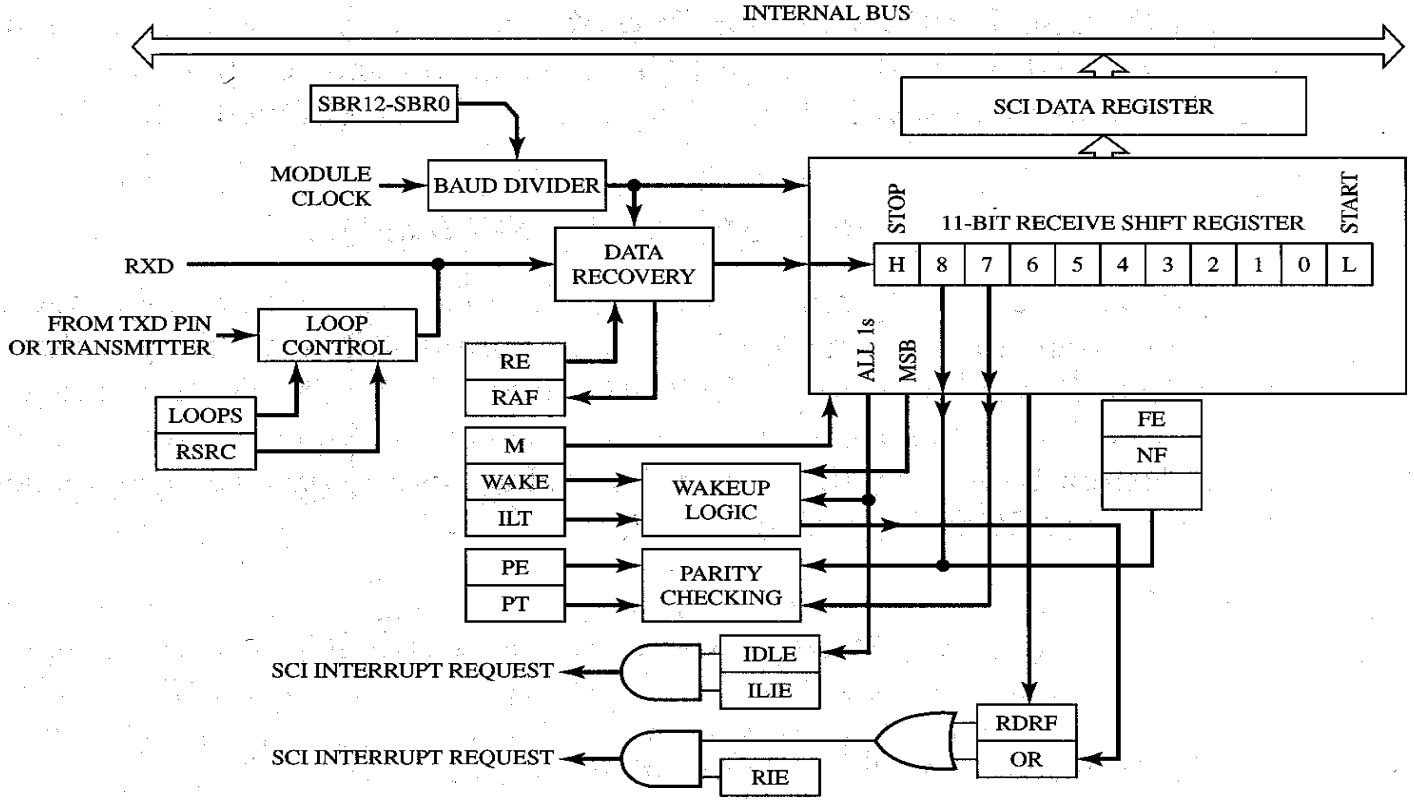


Figure 10.9 The SCI receiver. (Figure used with permission of Motorola, Incorporated.)

Serial Communications Interface (SCI) Registers

- SCI Baud Rate Control Registers
- SCI Control Registers 1, 2
- SCI Status Registers 1, 2
- SCI Data Registers High/Low

SCI Baud Rate Control Registers

Desired SCI Baud Rate	BR Divisor for M = 4.0 MHz	BR Divisor for M = 8.0 MHz
110	2273	4545
300	833	1667
600	417	833
1200	208	417
2400	104	208
4800	52	104
9600	26	52
14400	17	35
19200	13	26
38400	--	13

Register: SCI Baud Rate Control Register (SC0BDH/SC1BDH) Address: $00C0/$00C8

7	6	5	4	3	2	1	0
BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8
Reset: 0	0	0	0	0	0	0	0

Register: SCI Baud Rate Control Register (SC0BDL/SC1BDL) Address: $00C1/$00C9

7	6	5	4	3	2	1	0
SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Reset: 0	0	0	0	0	1	0	0

SCI Control Registers 1, 2

Register: SCI Control register 1 (SC0CR1/SC1CR1) Address: $00C2/$00CA

7	6	5	4	3	2	1	0
LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
Reset: 0	0	0	0	0	0	0	0

Register: SCI Control register 2 (SC0CR2/SC1CR2) Address: $00C3/$00CB

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset: 0	0	0	0	0	0	0	0

SCI Status Registers 1, 2

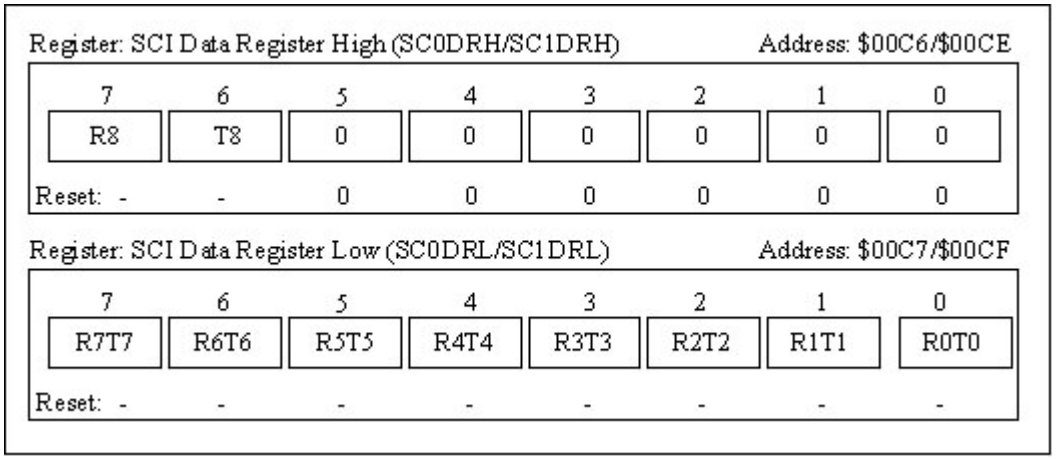
Register: SCI Status register 1 (SC0SR1/SC1SR1) Address: $00C4/$00CC

7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Reset: 1	1	0	0	0	0	0	0

Register: SCI Status register 2 (SC0SR2/SC1SR2) Address: $00C5/$00CD

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RAF
Reset: 0	0	0	0	0	0	0	0

SCI Data Registers High/Low



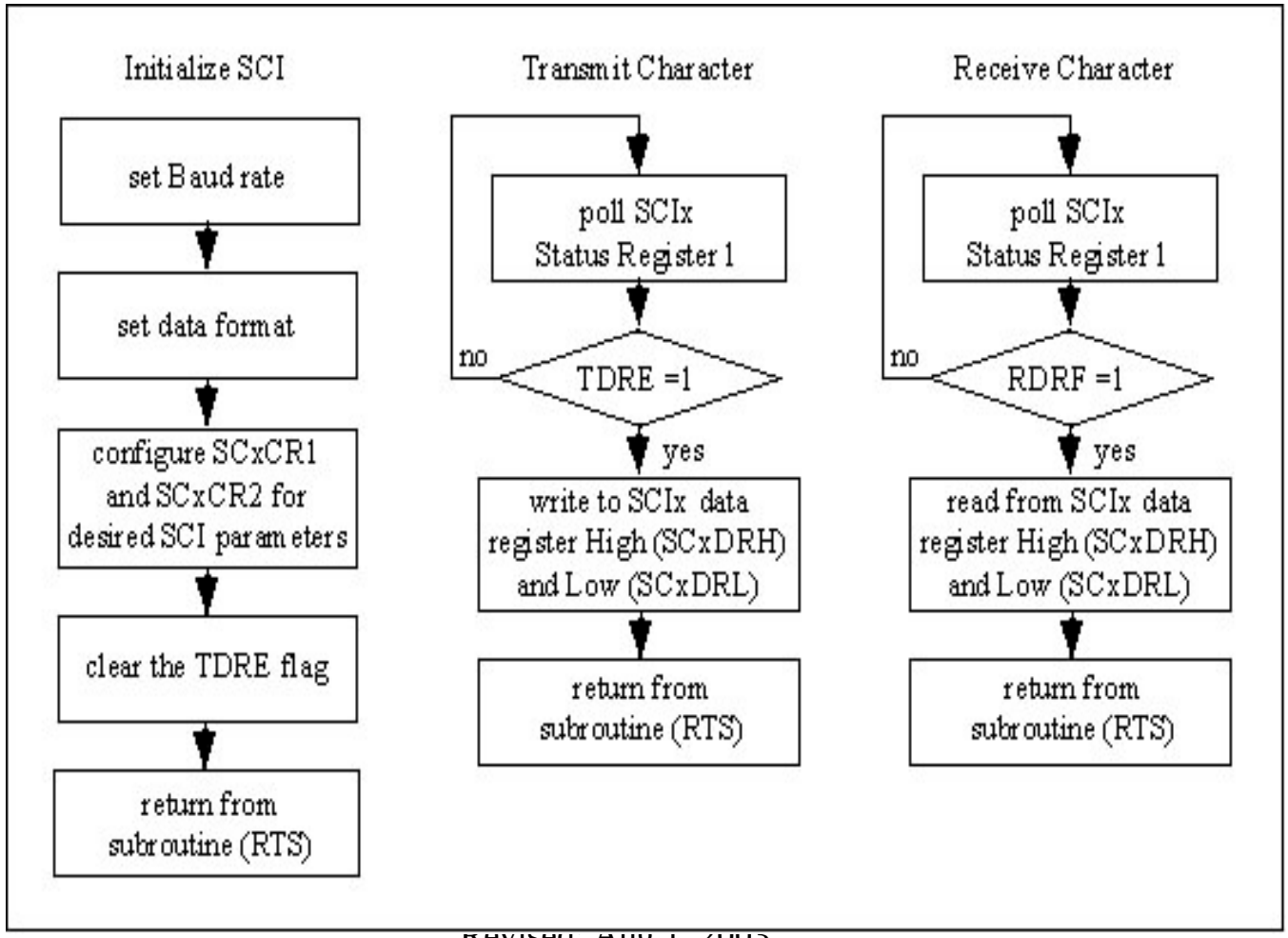
Register: SCI Data Register High (SC0DRH/SC1DRH) Address: $00C6/$00CE

7	6	5	4	3	2	1	0
R8	T8	0	0	0	0	0	0
Reset: -	-	0	0	0	0	0	0

Register: SCI Data Register Low (SC0DRL/SC1DRL) Address: $00C7/$00CF

7	6	5	4	3	2	1	0
R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
Reset: -	-	-	-	-	-	-	-

SCI Programming



Example

EX] Write a subroutine to initialize the SCI.
Assume the MCLK = 8 MHz and the data rate is 9600 BAUD.

- Configure SC1BDL, BDH
- Configure SC1CR1
- Configure SC1CR2
- Clear the TDRE flag in SC1SR1 - two step process:
  - Read SC1SR1
  - Write to SC1DR

Example (cont)

SC1BDH, SC1BDL:

SC1BDH = $00

SC1BDL = $34

SC1CR1:

M=0, (1 start, 1 stop,

8 data bits)

SC1CR2:

TE = 1

Register: SCI Baud Rate Control Register (SC0BDH/SC1BDH) Address: $00C0/$00C8

7	6	5	4	3	2	1	0
BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8
Reset: 0	0	0	0	0	0	0	0

Register: SCI Baud Rate Control Register (SC0BDL/SC1BDL) Address: $00C1/$00C9

7	6	5	4	3	2	1	0
SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Reset: 0	0	0	0	0	1	0	0

Register: SCI Control register 1 (SC0CR1) Address: $00C2

7	6	5	4	3	2	1	0
LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
Reset: 0	0	0	0	0	0	0	0

Register: SCI Control register 2 (SC0CR2/SC1CR2) Address: $00C3/$00CB

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset: 0	0	0	0	0	0	0	0

Register: SCI Status register 1 (SC0SR1/SC1SR1) Address: $00C4/$00CC

7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Reset: 1	1	0	0	0	0	0	0

Register: SCI Data Register Low (SC0DRL/SC1DRL) Address: $00C7/$00CF

7	6	5	4	3	2	1	0
R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
Reset: -	-	-	-	-	-	-	-

Example (cont)

```
;SCI Initialization Example
;Assume M = 8 MHz, 9600 BAUD

;define register locations and masks
SC1BDH = $00C8          ; Baud Register High location
SC1BDL = $00C9          ; Baud Register Low location
BAUD_HI = $00           ; Baud Register High mask
BAUD_LOW = $34          ; Baud Register Low mask
SC1CR1 = $00CA          ; Control Register 1 location
SC1_CONT = $00          ; Control Register 1 mask
SC1CR2 = $00CB          ; Control Register 2 location
SC1_MASK = $08          ; Control Register 2 mask
SC1SR1 = $00CC          ; Status Register 1 location
SC1DRL = $00CF          ; Data Register Low location
```

Example (cont)

```
;SCI Initialization Example
;Assume M = 8 MHz, 9600 BAUD

            .area sci_test(abs)         ; define name of absolute area
            .org $4000

_main::
            JSR     sci_init
            :
            :
            swi
```

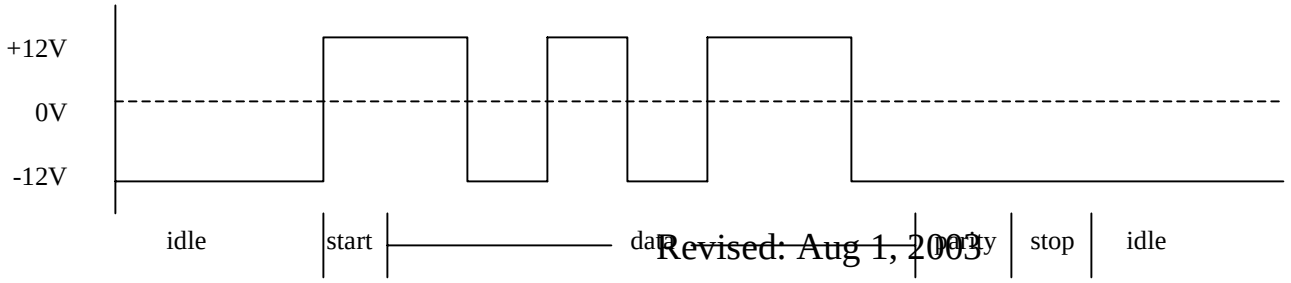
Example (cont)

```
;sci_init: initializes SCI system
;Assume M = 8 MHz, 9600 BAUD

sci_init::  LDAA    #BAUD_LOW       ;set BAUD rate
            STAA    SC1BDL
            LDAA    #BAUD_HI
            STAA    SC1BDH
            LDAA    #SCI_CONT       ;set MODE
            STAA    SC1CR1
            LDAA    #SC1_MASK       ;enable transmitter
            STAA    SC1CR2
            LDAA    SC1SR1          ;clear TDRE bit - 2 step process
            STAA    SC1DRL          ;1: read SC1SR1, write SC1DRL
            RTS                     ;return from subsroutine
```

RS-232 Standard

- Electronic Industry Association (EIA) Standard
- Evolved from 1960 standard - EIA-232-D
- Four aspects:
  - Electrical specifications: voltage level, rise time, fall time
  - Functional specifications of each signal
  - Mechanical specifications: number of pins, connector shape, connector dimension
  - Procedural specifications
- RS-232 voltage levels



RS-232 Standard (cont)