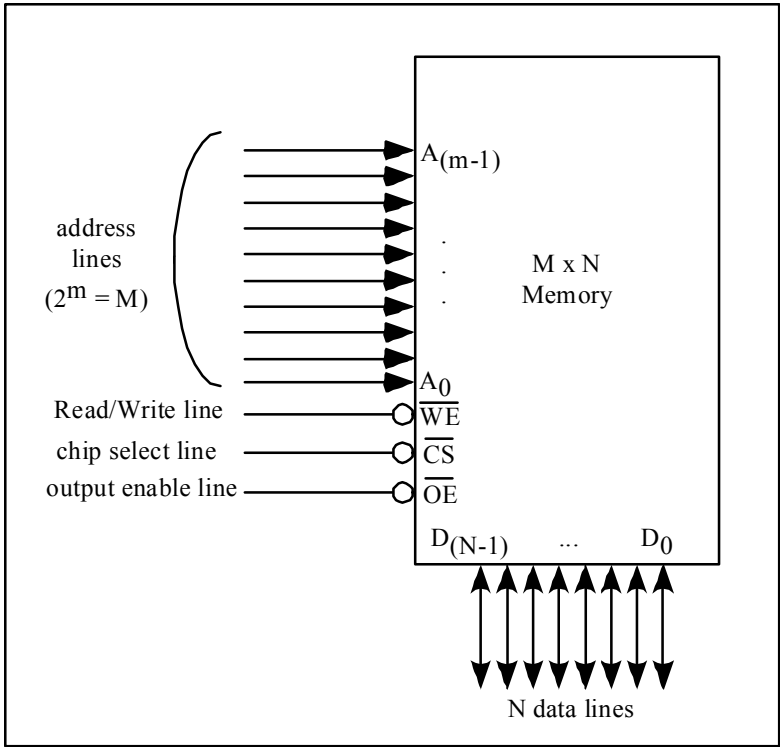
EE4800/EE5880
Real Time Embedded Systems

Lessons 15 - 17
Memory Expansion

Overview

- Basic memory concepts
- Memory expansion
  - Linear and Paging techniques
- Guidelines
- Detailed memory expansion design techniques
  - Layout
  - Control signals
  - Timing issues

Basic Memory Concepts capacity and control signals



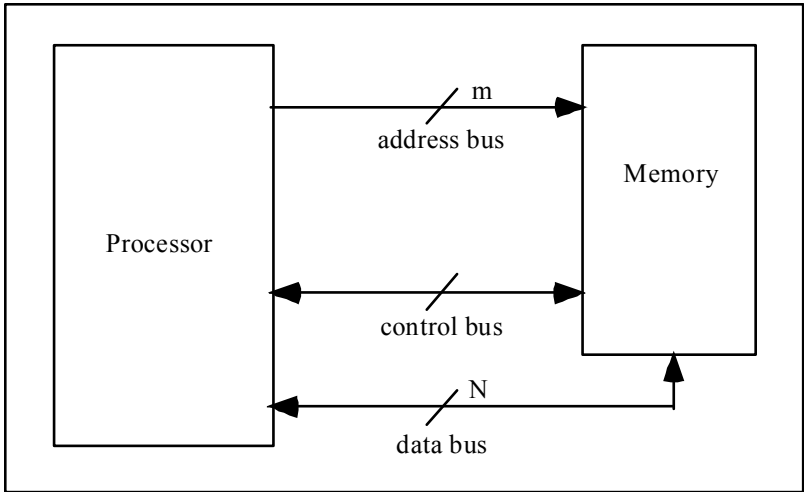
Basic Memory Concepts
control signals

- /WE: write enable - when activated values on data lines are written to specified address
- /OE: output enable - data at specified location placed on data pins of memory chip, data lines connected to data bus using tristate outputs
- /CS: chip select - used to select a specific chip in memory array

Basic Memory Concepts
memory buses

- address bus

$2^{\text{addr lines}} = \text{addr locations}$

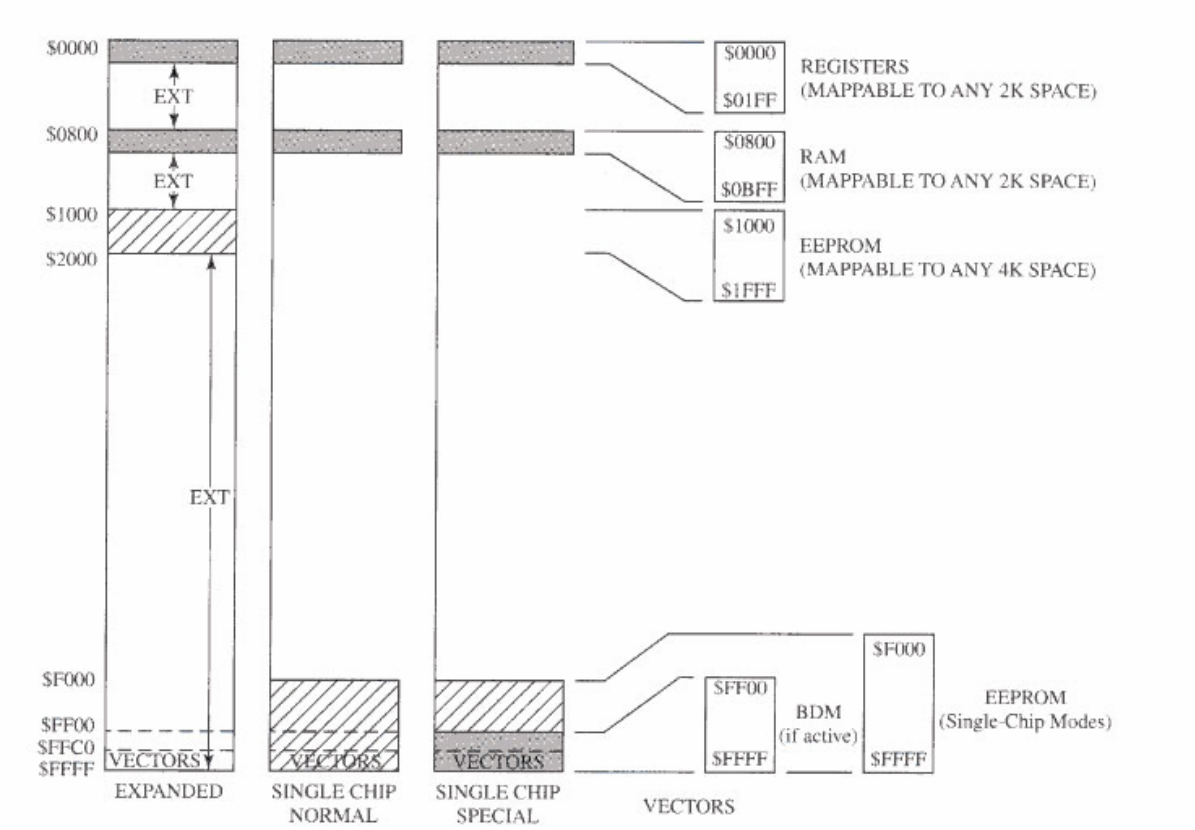


- data bus
- control bus

Basic Memory Concepts
RAM vs ROM

- RAM
  - read/write
  - volatile
  - faster access time
  - variants
    - SRAM
    - DRAM
  - applications
    - variables
    - dynamic memory allocation
      - heaps, stacks
- ROM
  - read only
  - non-volatile
  - slower
  - variants
    - ROM, PROM, EPROM, EEPROM (byte-addressable, FLASH)
  - applications
    - programs
    - constants, codes, etc.

Basic Memory Concepts
memory map



Memory Expansion

- Linear vs Paging
- Guidelines:
  - Unique address for each location
  - Data bus connected properly to all memory chips
  - Control lines routed to individual memory chips
  - Control signal timing are compatible between 68HC12 and external memory chips
  - External memory chips electrically compatible with 68HC12

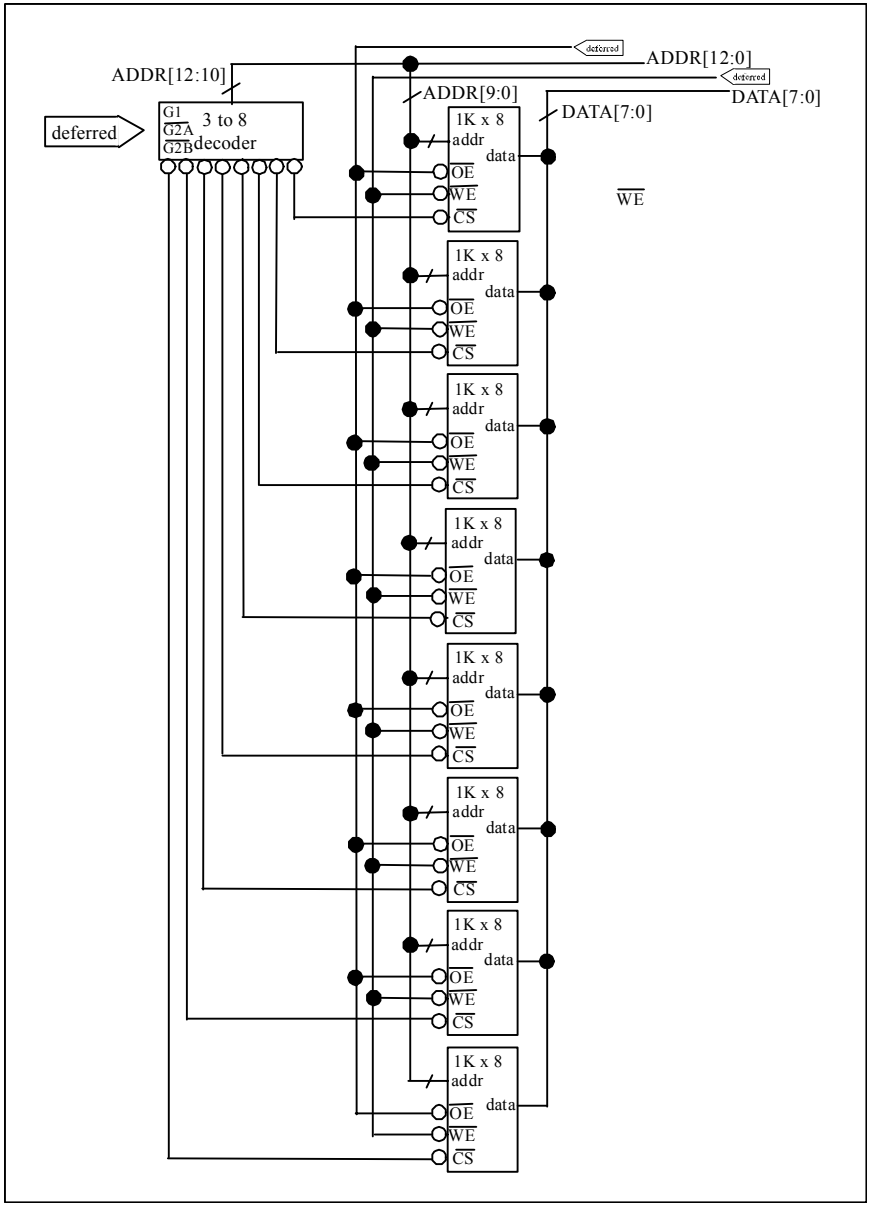
Memory Expansion Overview

- Memory layout design
  - Based on Dr. Jerry Cupal's techniques
- Control signals
  - 68HC12
  - external memory components
- Timing compatibility

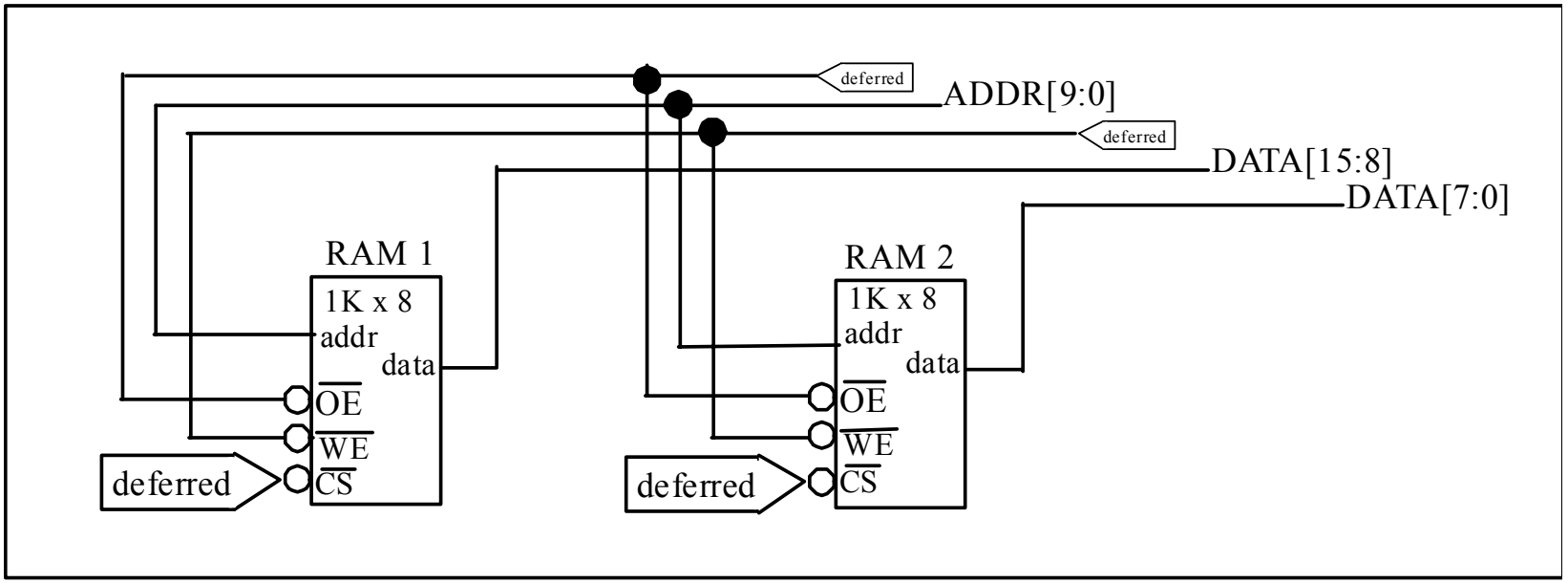
Memory Expansion layout design

- From system requirements determine amount of external devices needed
- Draw the desired memory table and design the address decoding and control logic
- Draw the schematic of the circuit
- Verify the design

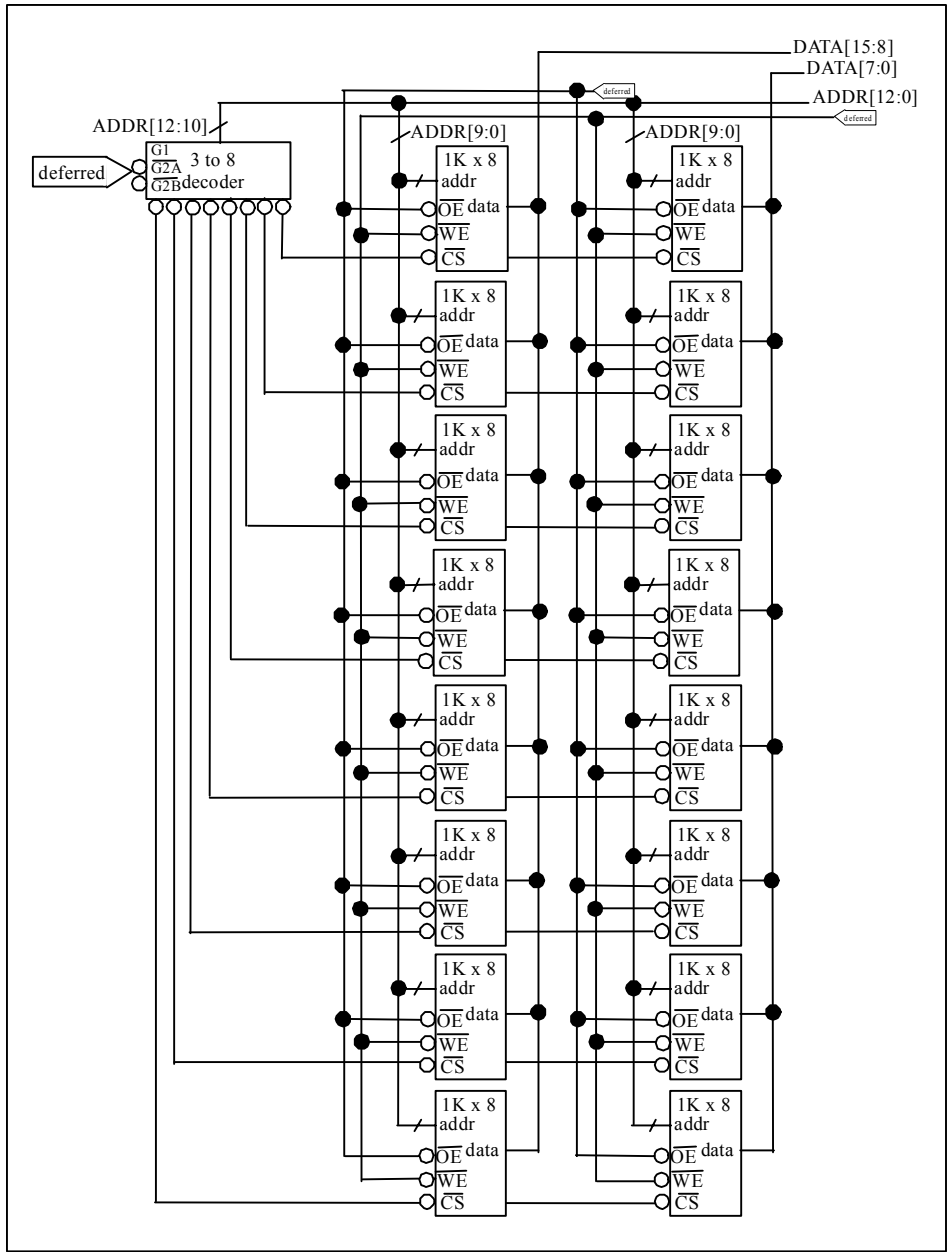
Memory Expansion expanding memory length



Memory Expansion
expanding memory width



Memory Expansion expanding memory length and width

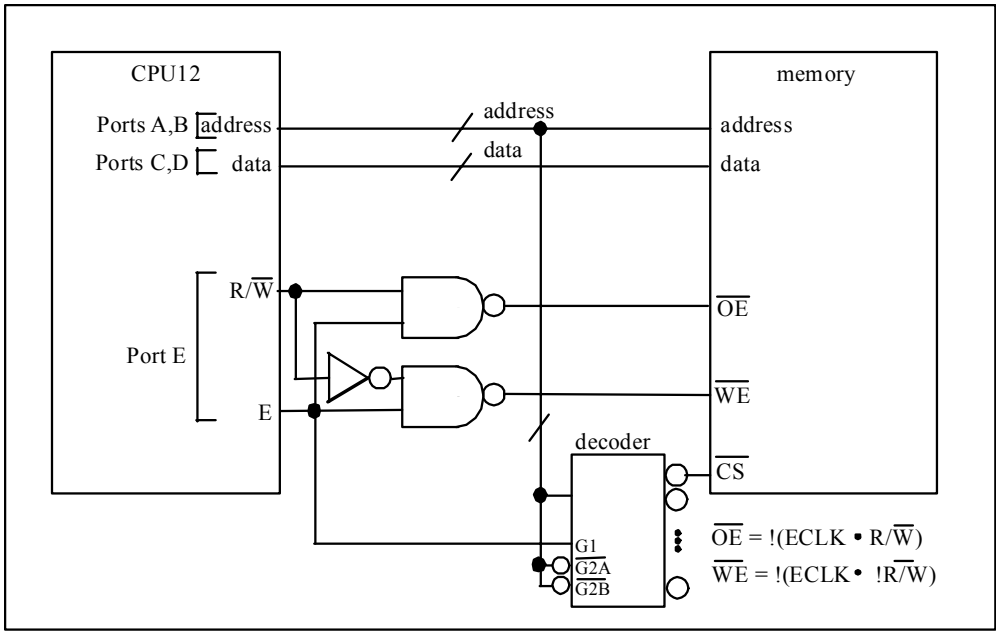


Memory Expansion memory table

Device	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Useable Locations
RAM0	0	0	1	0	0	0	●	●	●	●	●	●	●	●	●	●	$2000 - $23FF
RAM1	0	0	1	0	0	1	●	●	●	●	●	●	●	●	●	●	$2400 - $27FF
RAM2	0	0	1	0	1	0	●	●	●	●	●	●	●	●	●	●	$2800 - $2BFF
RAM3	0	0	1	0	1	1	●	●	●	●	●	●	●	●	●	●	S2C00 - $2FFF
RAM4	0	0	1	1	0	0	●	●	●	●	●	●	●	●	●	●	$3000 - $33FF
RAM5	0	0	1	1	0	1	●	●	●	●	●	●	●	●	●	●	$3400 - $37FF
RAM6	0	0	1	1	1	0	●	●	●	●	●	●	●	●	●	●	$3800 - $3BFF
RAM7	0	0	1	1	1	1	●	●	●	●	●	●	●	●	●	●	S3C00 - $3FFF

Memory Expansion control signals

- 68HC12 control signals
  - ECLK: basic bus clock
  - R/$\overline{W}$: indicates data direction
- Memory chips control signals
  - /WE: write enable
  - /OE: output enable
  - /CS: chip select



Memory Expansion timing analysis overview

- Must analyze timing compatibility between processor and memory
- Must analyze:
  - RAM
    - read cycle
    - write cycle
  - ROM
    - read cycle

Memory Expansion
timing analysis - RAM read cycle

- A valid address is placed on address lines ADDR[15:0]
- Control signals are issued by 68HC12
  - ECLK and R/$\overline{W}$
- Provides control inputs to memory components
  - /CS and /OE
- Data are read from the external memory by 68HC12

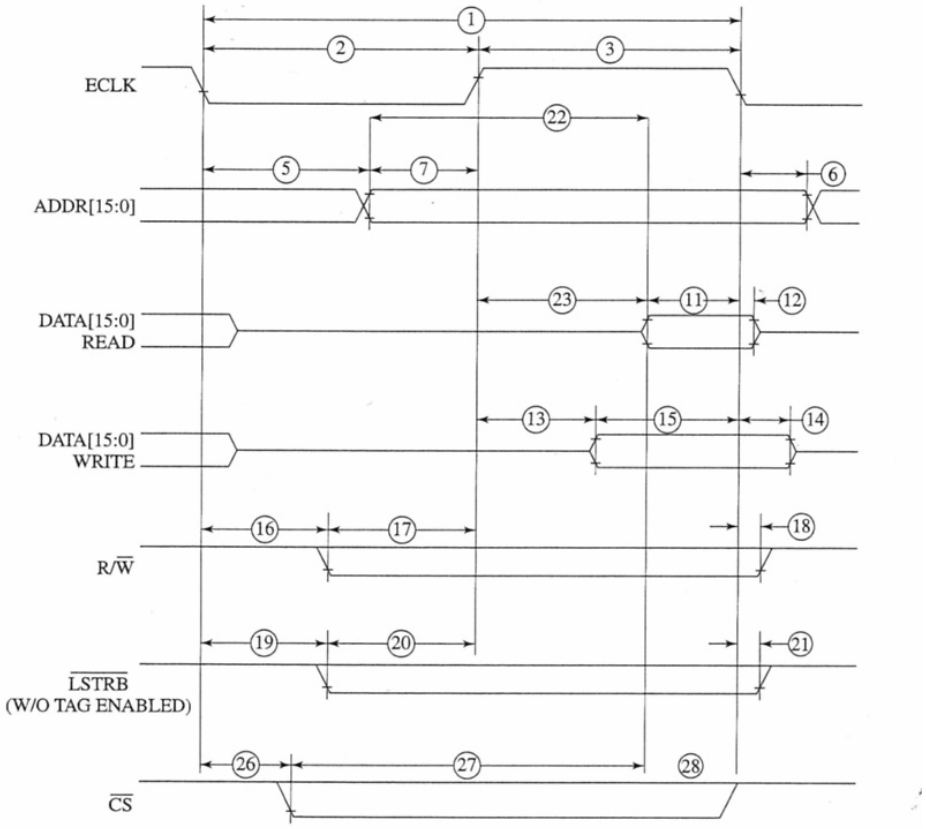
Memory Expansion
timing analysis - nonmultiplexd expansion bus timing

Num	Characteristic[1], [2]		Delay	Symbol	5 MHz Min	5 MHz Max	Unit
	Frequency of operation (E-clock frequency)		—	f_0	dc	8.0	MHz
1	Cycle time	$t_{cyc} = 1/f_0$		t_{cyc}	125	—	ns
2	Pulse width, E low	$PW_{EL} = t_{cyc}/2 + delay$	−2	PW_{EL}	60	—	ns
3	Pulse width, E high[3]	$PW_{EH} = t_{cyc}/2 + delay$	−2	PW_{EH}	60	—	ns
5	Address delay time	$t_{AD} = t_{cyc}/4 + delay$	29	t_{AD}	—	60	ns
6	Address hold time		—	t_{AH}	20	—	ns
7	Address valid time to E rise	$t_{AV} = PW_{EL} - t_{AD}$	—	t_{AV}	0	—	ns
11	Read data setup time		—	t_{DSR}	30	—	ns
12	Read data hold time		—	t_{DHR}	0	—	ns
13	Write data delay time	$t_{DDW} = t_{cyc}/4 + delay$	25	t_{DDW}	—	46	ns
14	Write data hold time		—	t_{DHW}	20	—	ns
15	Write data setup time[3]	$t_{DSW} = PW_{EH} - t_{DDW}$	—	t_{DSW}	30	—	ns
16	Read/write delay time	$t_{RWD} = t_{cyc}/4 + delay$	18	t_{RWD}	—	49	ns
17	Read/write valid time to E rise	$t_{RWV} = PW_{EL} - t_{RWD}$	—	t_{RWV}	20	—	ns
18	Read/write hold time		—	t_{RWH}	20	—	ns
19	Low strobe delay time	$t_{LSD} = t_{cyc}/4 + delay$	18	t_{LSD}	—	49	ns
20	Low strobe valid time to E rise	$t_{LSV} = PW_{EL} - t_{LSD}$	—	t_{LSV}	11	—	ns
21	Low strobe hold time		—	t_{LSH}	20	—	ns
22	Address access time[3]	$t_{ACCA} = t_{cyc} - t_{AD} - t_{DSR}$	—	t_{ACCA}	—	35	ns
23	Access time from E rise[3]	$t_{ACCE} = PW_{EH} - t_{DSR}$	—	t_{ACCE}	—	30	ns
26	Chip-select delay time	$t_{CSD} = t_{cyc}/4 + delay$	29	t_{CSD}	—	60	ns
27	Chip-select access time[3]	$t_{ACCS} = t_{cyc} - t_{CSD} - t_{DSR}$	—	t_{ACCS}	—		ns
28	Chip-select hold time		—	t_{CSH}			ns
29	Chip-select negated time	$t_{CSN} = t_{cyc}/4 + delay$	5	t_{CSN}			ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. All timings are calculated for normal port drives.
3. This characteristic is affected by clock stretch.
   Add N × t_{cyc} where N = 0, 1, 2, or 3, depending on the number of clock stretches.

Figure 8.15 Nonmultiplexed expansion bus timing definitions. (Figure used with permission of Motorola, Incorporated.)

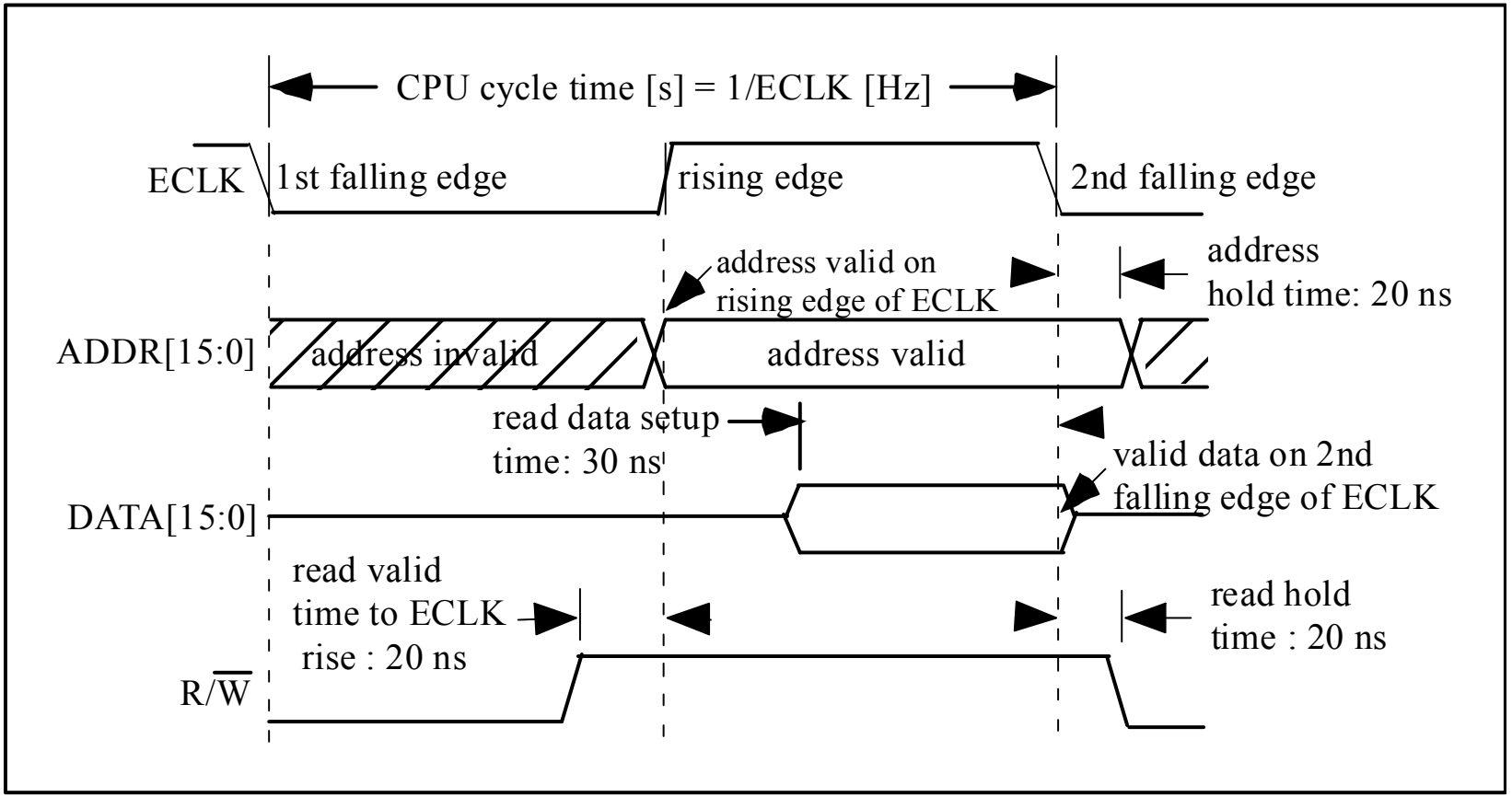
Memory Expansion
timing analysis - nonmultiplexd expansion bus timing



Note: Measurement points shown are 20% and 70% of V_{DD}.

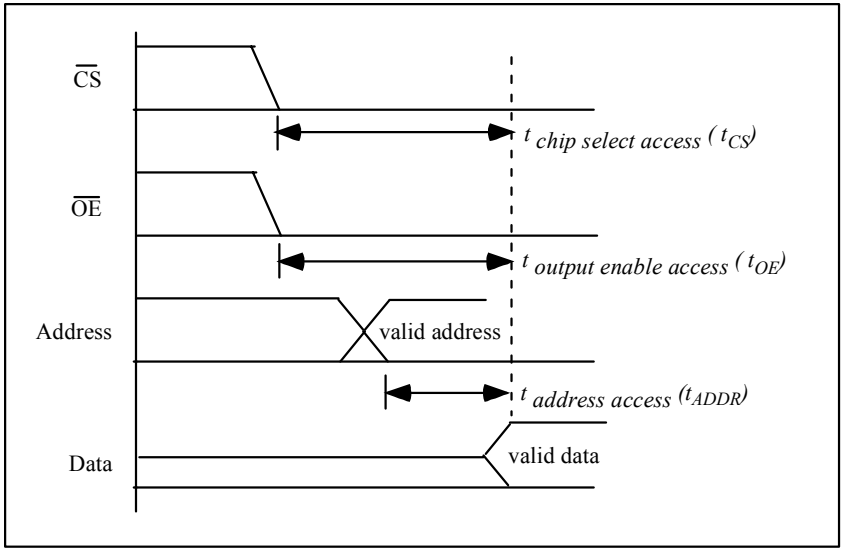
Figure 8.16 Nonmultiplexed expansion bus timing diagram. (Figure used with permission of Motorola, Incorporated.)

Memory Expansion
timing analysis - simplified timing diagram



Memory Expansion
timing analysis - timing signals

- Chip select access time (t_{CS})
- Address access time (t_{ADDR})
- Output enable access time (t_{OE})



Memory Expansion
four key questions

- **Q1:** How soon can valid data be provided by the SRAM memory chip after a chip select signal is provided by the 68HC12 under worst-case conditions?
- **Q2:** How soon can valid data be provided by the memory chip after a valid address is provided under worst-case conditions?
- **Q3:** How soon can valid data be provided to the 68HC12 once the memory chip has received a valid output enable signal?
- **Q4:** Final analysis - choose worst case situation