COLLEGE OF **ENGINEERING** &
APPLIED SCIENCE
UNIVERSITY OF WYOMING

Hardware Descriptive Language (HDL) Digital Design

EE 4490 Course Syllabus for Fall 2018

Abstract

This course introduces more advanced digital system designs (going beyond those of EE 2390), including design aspects related to modern computer architecture. The use of professional-level design tools and Verilog HDL is emphasized.

Contents

1 Instructor

Cameron H. G. Wright, Ph.D., P.E.
Office: EN 5052
Phone: 307-766-6104
E-mail: `chgw@uwyo.edu` (preferred contact method)
Office hours: Mon through Fri: 11:00 AM–12:00 PM

2 Course Goals and Objectives

Goal: The goal of this course is for the students to further develop the ability to analyze an existing digital circuit or to synthesize a new digital design to meet stated specifications, using professional-level design tools and Verilog HDL.

Objectives: Students will be able to

- Correctly describe the detailed behavior of given digital logic circuits as defined by Verilog HDL, state diagrams, or other means, including those circuits related to modern computer architecture.
- Translate system requirements into a practical digital design, making use of modern engineering tools such as Xilinx Vivado, Verilog HDL, and FPGA prototyping boards.
- Demonstrate the ability to modify existing HDL code to meet new system requirements.
- Demonstrate hands-on test bench and prototyping skills to ensure that a design meets the specified system requirements.

3 Course Prerequisites

The student must have satisfactorily completed EE 2390 or equivalent. If you are in this course without the appropriate prerequisites, you will be administratively dropped. This may happen immediately, but it can occur at any time during the semester if you are found to not have the prerequisites. This is a College-wide policy regarding prerequisites.

4 Course Grading

4.1 Breakdown of Graded Events

Graded material is given the weights shown in the following table. Note that the Final Exam is scheduled from 1:15 PM to 3:15 PM on Thursday, December 13, 2018 in our regular classroom. The Final Exam is **optional**; it can be used to possibly improve your semester exam average. The semester exams and Final Exam will all be given equal weight.

	Weight
Exams (2 during semester, optional final exam)	50% (total, individual effort)
Projects	30% (team effort)
Homework	15% (individual effort)
Quizzes	5% (individual effort)
Total	100%

The frequency of homework assignments and quizzes will be determined by the apparent mastery of topics by the students, but will occur no more than weekly. Solutions to the homework may be posted on the EE 4490 WyoCourses website *after* the turn-in deadline. In most cases, just one randomly selected part of a given homework assignment will be graded, and this makes up one-half of the total score for the assignment. The remaining part(s) from the assignment will be "spot checked" for a reasonable effort, and this makes up the other half of the total score for the assignment.

Quizzes and exams will typically be given during normal class time; however, take-home quizzes and/or exams are a possibility. For "in-class" quizzes and exams, only a pencil and calculator are allowed; no mobile devices (phones, tablets, etc.) may be used and must be put away out of sight. Typically, an acceptable engineering lab notebook created by the student is also allowed for "in-class" quizzes and exams. More details will be announced in class.

Unless arranged for *ahead of time* by the student with the instructor, it is *not possible* to make up a missed exam or quiz without an Authorized Absence (available only from the Dean of Students Office). This policy, in accordance with University Regulation 2-108, is strictly observed. See `http://www.uwyo.edu/dos/absences/`.

4.2 Grading Scale

The course will be graded on the following scale, where the student's overall average in the course, as a percentage, is represented by x. No "curving" for grades is used.

Grade	Average (%)
A	$90 \leq x \leq 100$
B	$80 \leq x < 90$
C	$70 \leq x < 80$
D	$60 \leq x < 70$
F	$0 \leq x < 60$

4.3 Turn-In Policy

All homework assignments are due at the *beginning* of the lecture period on the associated due date. Students should use the unlined side of standard *engineering paper* to neatly record their homework solutions. Computer printouts may also be used if appropriate. Be sure that you write your name and HW assignment number neatly at the top of each page; multiple pages should be stapled together (no paper clips or cute little folds—this isn't grade school!). Be sure to write clearly and neatly, show all of your solution process, and clearly indicate your final answers by underlining them or drawing a box around them

(or simply annotating if appropriate). I will *not* attempt to decipher messy or inscrutable handwriting; you could end up with a zero if your homework is difficult to read.

Project turn-in requirements will vary by project and will be listed as part of the individual project instructions. Projects may also require a demonstration to your instructor; plan ahead for that.

Late turn-ins will not be accepted unless an extraordinary situation exists. Very few circumstances constitute an extraordinary situation—so plan ahead!

5 Course Materials and Resources

5.1 Textbook

Our textbook, by Harris and Harris, is listed as [1] in the References section of this syllabus. This book provides good coverage of the topics, and emphasizes modern design methods. In this course, we will cover material from approximately the second half of the book (i.e., most of Chap. 6–8), with supplementary notes supplied as needed for certain topics (note that the first half of this book is typically used for EE 2390). Take advantage of the many examples in the book.

5.2 eBooks

While the price of the textbook is quite reasonable compared to most engineering texts, if you are a fan of electronic books (eBooks) you can access various other related textbooks and references for free here at UW. A very rich collection of textbooks in electronic form can be accessed through the University of Wyoming Library online eBook facility.

For example, the textbooks listed in the References section of this syllabus as [2, 3, 4, 5, 6] provide reasonable discussions of the majority of the fundamentals of digital system design. Note that [2] is *very* similar to your textbook, except that it explains the classic MIPS computer architecture instead of the more popular ARM computer architecture. For EE 4490, books [1] and [2] are significantly different due to the different computer architectures that are covered. Other well-known computer architecture books such as [7, 8, 9] may have earlier editions available as eBooks, and the latest editions can be rented from the publisher. The texts listed as [10, 11, 12] are excellent references for the use of the Verilog HDL (hardware description language). Regarding Verilog books, be careful about which version of Verilog is covered in the book. While Verilog and SystemVerilog merged to some degree in 2009 as IEEE Standard 1800-2009, Verilog is still widely used by itself (IEEE Standard 1364-2005). In this course, we will use Verilog.

Additional references pertinent to this course are also listed in the References section of this syllabus; they may or may not be available as eBooks.

5.3 Lecture Slides

Extensive lecture slides will be used throughout the course that will cover all the topics discussed in class. Copies of these slides will be available on the course website.

5.4 Online Resources

We will make frequent use of the course website hosted under the WyoCourses system. It is a secure web host for UW students, and you will need to log in with your normal UW student account details. **We will mainly use just the "Files" area of the website.** A copy of this syllabus, lecture slides, homework assignments, homework solutions, and other supplemental material will be posted to this web site. **You are responsible for checking it regularly.** Files will be organized using easy-to-understand subdirectory and file names. Many course materials will also be available on the ECE Department network drive that can be found at `\\warehouse\ece\EE4490`.

Another web site you may find helpful is the companion website for your textbook, maintained by the publisher. You can use the URL listed in the book's Preface (see p. xxi) or the more direct URL given below.

`http://booksite.elsevier.com/9780128000564/`

This is a richly populated web site with solutions to odd-numbered problems, all the figures in the book, additional chapters, errata for the text, etc. You are encouraged to take advantage of it!

5.5 Required Software and Other Resources

All software described here is freely available online. To complete the projects, each student must become adept at using a professional-grade software package for digital design. The primary software used in this course is:

- **Xilinx Vivado WebPACK (2017.2 version or newer).** This software is already installed on ECE Dept computers (ECE Digital Lab, EN 5030 and ECE Computer Lab, EN 5038). If you wish to have your own copy (the WebPACK is free), the download is rather large (roughly 7.6 GB), and you'll encounter several installation questions (e.g., product registration and license manager installation) if you choose to proceed. The process begins at `http://www.xilinx.com/`.

Another very nice software tool that *is needed to solve some homework problems* and also allows easy practice using Verilog to create and test various digital designs is:

- **Icarus Verilog and GTKWave:** These free programs provide a lightweight, clean, and simple *command-line* Verilog compiler, simulator, and waveform viewer. This tool is *much* smaller, simpler, and faster to use than the Xilinx Vivado program! It's available for Windows, Linux and Mac OS X. Use a Google search for your preferred platform download. A Windows compatible install file for these two tools is available on the course website and also on the ECE Department network drive mentioned above; for both locations, look in the `Install_Verilog` directory.[1]

[1] You may also want to explore other tools, such as the free online Verilog compiler that is part of the website called EDA Playground at `https://www.edaplayground.com/`. But you'll still need Icarus Verilog and GTKWave.

- **Required FPGA Board:** Some of the homework and all of the projects require the use of an inexpensive student-owned "Basys 3 Artix-7 FPGA Trainer Board" manufactured by Digilent, Inc. This is the same board that is used for EE 2390. See `https://store.digilentinc.com/` for details. The Basys 3 board is a circuit design and implementation platform for digital circuits. Built around a Xilinx Artix-7 Field Programmable Gate Array (FPGA), the Basys 3 board provides a complete, ready-to-use hardware (and firmware) platform suitable for implementing a wide variety of digital designs. A large collection of on-board I/O devices and all required FPGA support circuits are included on the board, and it easily connects to your computer via a USB port. **Each student must have purchased their own Basys 3 board in time to have it in hand very early in the semester.** While the list price is $149.00, if you proceed through the Digilent Store Academic Verification for Students process, you can reduce that cost to $111.75 (as of this writing). You'll also need the appropriate USB cable (USB A to micro-B), which is does not come with the board. You can get this from Digilent or any other vendor, typically for less than $5.

6 Miscellaneous Course Policies

6.1 Collaboration, Attendance, and Student Behavior Policy

To solve the homework assignments, you are encouraged to work with other students currently enrolled in EE 4490. **Don't try to use, and most certainly don't copy, homework solutions from previous semesters.** Not only is it academically dishonest to do so, but a very subtle change in the assignment can cause significant changes in the correct solution. It is *very obvious* when a student turns in a solution to a previous semester's assignment.

For allowed collaborations, you must document *any* of the help you receive in the form of comments directly on your homework paper as appropriate. No comments mean you are submitting the item as *totally* your own work; my assumption will always be that you are an honorable person unless you cause me to believe otherwise. Simply copying another person's work is, of course, not allowed—the actual item you turn in must ultimately be your own work. You may be called into my office with no advance notice to explain, in detail, the specifics of your solution.

Quizzes and exams must always be the *student's own work*, with no collaboration, even if given as a "take-home" event.

Attendance for class lectures is left to the student's own (hopefully mature) judgment. While the lesson slides and textbook provide the main concepts, lectures provide considerable amplification, explanation, and overall context of the concepts, and therefore should not be missed. And if you miss class, you'll miss my immensely funny jokes!

Student behavior is expected to always be professional and respectful of others. An enduring goal is to foster a positive learning environment for all. Side conversations, and the use of cell phones or other mobile devices in such a way that it distracts others, is strictly forbidden during class.

6.2 Academic Honesty

"The University of Wyoming is built upon a strong foundation of integrity, respect and trust. All members of the University community have a responsibility to be honest and have the right to expect honesty from others. Any form of academic dishonesty is unacceptable to our community and will not be tolerated." [excerpted from the UW General Bulletin] All persons should report suspected violations of standards of academic honesty to the instructor, department head, or dean. See UW Regulation 2-114, "Procedures and Authorized University Actions in Cases of Student Academic Dishonesty." You can read this and all other University regulations at: `http://www.uwyo.edu/regs-policies/`

6.3 Disability and Diversity Statements

If you have a physical, learning, sensory, or psychological disability and require accommodations, please let the instructor know as soon as possible. You must register with, and provide documentation of your disability to, Disability Support Services (DSS) located in room 128 of Knight Hall. You may also contact DSS at (307) 766-3073 or `udss@uwyo.edu`. Visit their website for more information: `www.uwyo.edu/udss`.

From UW Regulation 2-117: "The University of Wyoming values an educational environment that is diverse, equitable, and inclusive. The diversity that students and faculty bring to class, including age, country of origin, culture, disability, economic class, ethnicity, gender identity, immigration status, linguistic, political affiliation, race, religion, sexual orientation, veteran status, worldview, and other social and cultural diversity is valued, respected, and considered a resource for learning."

7 Course Overview

Welcome to EE 4490! This course will prepare you to go beyond the digital system design challenges most of you encountered in EE 2390, and help you to take on new challenges that are similar to those likely to be encountered in industry. The emphasis in EE 4490, just as it was in EE 2390, is on fundamental principles and practical applications, rather than esoteric theory or arcane derivations.

Verilog HDL, more advanced than what you saw in EE 2390, is a central part of the course, and one of the vehicles we use to explore its capabilities is modern computer architecture to include assembly and machine language, the ALU, pipelines, memory configurations, and so forth. We will discuss the general case, and also examine specifics found in the extremely popular ARM microprocessor.

We will discuss other digital systems as appropriate, and may build off of lab exercises from EE 2390 to allow mastery of common industry activities related to HDL design work, such as modification of legacy code.

Just like with anything worthwhile in life, if you aren't willing to put in the time and effort, you won't ever become good at it. Be prepared to devote considerable time and effort to this class. I promise to be sensitive to the time requirements of every assignment I give you, but *you* have to put forth the effort. As Robert E. Heinlein was known to say, "TANSTAFL." Do you know what that stands for?

Some recommendations for success in this class which you might want to consider...

Don't miss class. New material, some of which is not in the text, is covered each lecture. Attendance at lecture isn't required, but if you miss class, *you* are responsible for covering the missed material on your own.

Don't arrive late for class. Make a genuine effort to come to class on time. It's the courteous and adult thing to do. Arriving late is disruptive for other students (and for me).

Read in advance. The reading assignments are listed in the next section. Your textbook is quite readable, and you are *expected* to read it. Whining that "the book is too hard to read" receives very little respect in any forum.

Start homework and projects early. Give yourself enough time to consider the problems and determine whether or not you need assistance of another student or your instructor. Last-minute questions are a bad idea, and you probably won't like the answer.

Ask questions. This includes during class, during discussions, and during office hours. I don't like a silent class—feel free to ask questions or make reasonable comments at will (but please, no distracting side conversations).

Review lecture notes shortly after class. Numerous studies of human learning have shown that if you review lesson slides and any notes you took soon after class, it will help you far more than waiting to review just before a quiz or exam.

Don't "blow off" homework or quizzes. They comprise 20% of your grade!

Let's have fun in this class! I like lively, attentive, alert students with an active sense of humor. It's more fun that way for all of us...

8 Course Schedule

This is an approximate lesson-by-lesson schedule, *subject to change*. Significant changes to this schedule will be announced in class, sent via e-mail, and/or posted on the course website.

Week	Lecture Number	Date	Day of Week	Topic	Text Reading
1	1	30-Aug-2018	R	Introduction to Class, Begin Verilog Combinational Logic Review	
2	2	4-Sep-2018	T	Continue Verilog HDL Review	Ch. 4, pp. 173—209
	3	6-Sep-2018	R	Review HDL, Finite State Machines and Testbenches	Ch. 4, pp. 209—225
3	4	11-Sep-2018	T	Working with iverilog, GTKWave, Xilinx WebPack, and Basys 3	Notes
	5	13-Sep-2018	R	Project 1: timing, bitstreams, and LED lightshows	Notes
4	6	18-Sep-2018	T	Project 1: timing, bitstreams, and LED lightshows	Notes
	7	20-Sep-2018	R	Intro to Computer Architecture and Assembly Language	Ch. 6, pp. 295—303
5	8	25-Sep-2018	T	Machine Language, Instructions and Branching	Ch. 6, pp. 303—312
	9	27-Sep-2018	R	Looping, Arrays, Data Types	Ch. 6, pp. 312—317
6	10	2-Oct-2018	T	*instructor travel: ABET*	
	11	4-Oct-2018	R	Function Calls, Returns and the Stack	Ch. 6, pp. 317—329
7	12	9-Oct-2018	T	Machine Language	Ch. 6, pp. 329—338
	13	11-Oct-2018	R	**Exam #1**	
8	14	16-Oct-2018	T	Compiling, Linking, Loading, Odds and Ends	Ch. 6, pp. 339—360
	15	18-Oct-2018	R	Introduction to Microarchitectures, Single Cycle Processors	Ch. 7, pp. 385—406
9	16	23-Oct-2018	T	Multicycle Processors	Ch. 7, pp. 406—425
	17	25-Oct-2018	R	Pipelined Processors	Ch. 7, pp. 425—443
10	18	30-Oct-2018	T	HDL Single-Cycle Processor Design	Ch. 7, pp. 443—456
	19	1-Nov-2018	R	HDL Single-Cycle Processor Continued	Notes
11	20	6-Nov-2018	T	Project 2: create your own ARM microprocessor	Notes
	21	8-Nov-2018	R	Project 2: create your own ARM microprocessor	Notes
12	22	13-Nov-2018	T	Intro to Memory Systems, Caches	Ch. 8, pp. 487—508
	23	15-Nov-2018	R	Virtual Memory, I/O Systems	Ch. 8, pp. 508—519
13	24	20-Nov-2018	T	**Exam #2**	
	No Class	22-Nov-2018	R	**Thanksgiving Break, no classes**	
14	25	27-Nov-2018	T	Project 3: driving a VGA video display	Notes
	26	29-Nov-2018	R	Project 3: driving a VGA video display	Notes
15	27	4-Dec-2018	T	Advanced Topics	Notes
	28	6-Dec-2018	R	Advanced Topics	Notes
	Final Exam	13-Dec-2018	R	**Final Exam (1:15—3:15 pm)**	

References

[1] S. L. Harris and D. M. Harris, *Digital Design and Computer Architecture, ARM Edition*, Morgan Kaufmann Publishers, 2015. ANNOTATION: An excellent, succinct text that emphasizes the latest design methods, showing SystemVerilog and VHDL coding styles.

[2] D. M. Harris and S. L. Harris, *Digital Design and Computer Architecture*, Morgan Kaufmann Publishers, 2nd ed., 2013. ANNOTATION: Very similar to your texbook, this text covers MIPS instead of ARM architecture.

[3] B. Holdsworth and C. Woods, *Digital Logic Design*, Newnes Publishing, 4th ed., 2002.

[4] C. Maxfield, *Bebop to the Boolean Boogie: An Unconventional Guide to Electronics*, Newnes Publishing, 3rd ed., 2009. ANNOTATION: A truly great book! This book is fun to read; you can learn all about digital logic while being entertained by this talented author. Too bad it isn't quite suitable as a textbook, but you do get a good seafood gumbo recipe in the appendix!

[5] C. Maxfield, *The Design Warrior's Guide to FPGAs: Devices, Tools and Flows*, Newnes Publishing, 2004. ANNOTATION: Another great book by "Max" Maxfield! While more advanced than his "Boogie" book, this book is similarly fun to read; you can learn all about state-of-the-art programmable digital logic without getting bored. It's a quick and informative read.

[6] R. Kamal, *Digital Systems Principles and Design*. Pearson Education India, 2006.

[7] M. M. Mano, C. R. Kime, and T. Martin, *Logic and Computer Design Fundamentals*. Pearson, 5th ed., 2016. ANNOTATION: A very readable teatment of computer architecture, less detailed than the Patterson and Hennessy text.

[8] D. A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*. Morgan Kaufmann Publishers, 5th ed., 2014. ANNOTATION: A detailed teatment of computer architecture, and the tradeoffs between hardware and software, written by two of the most respected authors in the field. Master this one before taking on the even more detailed text by Hennessy and Patterson.

[9] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*. Morgan Kaufmann Publishers, 6th ed., 2019. ANNOTATION: A very detailed teatment of computer architecture, considered by many to be THE definitive text on the subject, written by two of the most respected authors in the field. This is an advanced text.

[10] R. B. Reese and M. A. Thornton, *Introduction to Logic Synthesis using Verilog HDL*. Morgan & Claypool Publishers, 2006. ANNOTATION: A very good book co-writtem by a friend of your professor. Note that a very large collection of Morgan & Claypool technical books, such as this one, are available to UW students free of charge.

[11] S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*. Prentice Hall PTR, 2nd ed., 2003. ANNOTATION: One of my favorite introductory Verilog books. Well written, very complete, and logically organized.

[12] P. J. Ashenden, *Digital Design: An Embedded Systems Approach Using Verilog*, Morgan Kaufmann Publishers, 2008.

[13] M. M. Mano and M. D. Ciletti, *Digital Design*. Prentice Hall, 5th ed., 2012. ANNOTATION: A very complete yet readable introductory text. Many excellent digital logic examples, but sometimes not the best treatment of Verilog HDL.

[14] J. F. Wakerly, *Digital Design: Principles and Practices, with Verilog*. Pearson, 5th ed., 2018. ANNOTATION: A densely written but extremely informative book on digital design. Considered by many to be one of the definitive texts on fundamental digital design, it is sometimes used for introductory courses but also is used in more advanced courses. An excellent reference book for your professional library, but rather expensive.

[15] B. J. LaMeres, *Introduction to Logic Circuits & Logic Design with Verilog*. Springer, 2017.

[16] V. Taraate, *Digital Logic Design Using Verilog*. Springer, 2016.

[17] J. Bhasker, *A Verilog HDL Primer*. Star Galaxy Publishing, 3rd ed., 2005. ANNOTATION: A very easy to read introduction to Verilog, but a bit on the elementary side. Based on the older Verilog 2001 Standard, and does not cover SystemVerilog.

[18] S. Sutherland and D. Mills, *Verilog and SystemVerilog Gotchas: 101 Common Coding Errors and How to Avoid Them*. Springer, 2007. ANNOTATION: Wow! This short, easy-to-read book can save you many hours of frustration! Highly recommended.

[19] K. Coffman, *Real World FPGA Design with Verilog*. Prentice Hall PTR, 2000. ANNOTATION: A bit advanced, but as the title says it is full of real-world practical tips. Uses an older form of Verilog, but still useful.

[20] M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*. Pearson/Prentice Hall, 2nd ed., 2010. ANNOTATION: An advanced but fairly well written text with lots of examples. Unfortunately, uses a dated treatment of Verilog

[21] R. Mehler, *Digital Integrated Circuit Design Using Verilog and SystemVerilog*. Newnes Publishing, 2015.

[22] Y. Li, *Computer Principles and Design in Verilog HDL*. John Wiley & Sons, 2015.

[23] M. D. Ercegovac and T. Lang, *Digital Arithmetic*. Morgan Kaufmann Publishers, 2004. ANNOTATION: A detailed treatment of all types of computer-based mathematics, number systems, and numerical representations.

Only one more page to go...

Finally. . .

Congratulations on reading this far! Lesser mortals gave up a page or two ago. As a reward, perhaps these quotes will inspire you in a positive manner. . .

One must learn by doing the thing; for though you think you know it, you have no certainty until you try it.
—Sophocles

Simplicity is the ultimate sophistication.
—Leonardo da Vinci

Science can amuse and fascinate us all, but it is engineering that changes the world.
—Isaac Asimov

I am not discouraged, because every wrong attempt discarded is another step forward.
—Thomas Edison

That which does not kill us makes us stronger.
—Friedrich Nietzsche