UNIVERSITY OF WYOMING

EE 2390 Digital Systems Design

Course Syllabus for Spring 2015

Abstract

This course introduces the fundamentals of digital systems design, including number systems, combinational and sequential digital logic, state machines, and modern programmable logic devices. The use of professional-level design tools, including schematic capture and Verilog HDL is emphasized.

Contents

1 Instructor

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2 Course Goals and Objectives

Goal: The goal of this course is for the students to develop the ability to analyze an existing digital circuit or to synthesize a new digital design to meet stated specifications.

Objectives: Students will be able to

- Work effectively with a variety of number systems and numeric representations, including signed and unsigned binary, hexadecimal, 2's complement, fixed point, and floating point.
- Apply fundamental analysis skills to correctly describe the detailed behavior of given combinational and sequential digital logic circuits.
- Translate system requirements into a practical digital design, making use of modern EDA tools such as schematic capture, Verilog HDL, and logic synthesis programs.
- Demonstrate hands-on test bench skills and the ability to communicate appropriately via a lab notebook while functioning as part of an engineering lab team.

3 Course Prerequisites

The student must have satisfactorily completed MATH 2205 *(Calculus II)*.

4 Course Grading

4.1 Breakdown of Graded Events

Graded material is given the following weights. Note that **the Final Exam is scheduled** from 10:15 AM to 12:15 PM on Friday, May 15, 2015.

	Weight
Exam 1	20%
Exam 2	20%
Final Exam	25%
Homework	10%
Quizzes	10%
Laboratory	15%
Total	100%

Typically there will be one homework assignment and at least one "in class" quiz each week. Solutions to the homework will be posted on the EE 2390 WyoCourses web site *after* the turn-in deadline. In most cases, just one randomly selected problem from a given homework assignment will be graded, and this makes up one-half of the total score for the assignment. The remaining problems from the assignment will be "spot checked" for a reasonable effort, and this makes up the other one-half of the total score for the assignment. Students are responsible for checking the web site to verify their own solutions to all homework problems; variations of homework problems sometimes show up on exams or quizzes!

Exams and quizzes will be given during normal class time; exams will have a 50-minute time limit. Only a pencil and calculator are allowed while taking an exam or quiz; no mobile devices (phones, tablets, etc.) may be used and must be put away out of sight. Typically, a note sheet is allowed for exams; details will be announced in class.

Unless arranged for *ahead of time* by the student with the instructor, it is not possible to make up a missed quiz or exam without a University Excused Absence (available from the Office of Student Life). This policy is strictly enforced.

4.2 Turn-In Policy

All homework assignments are due at the *beginning* of the lecture period on the associated due date. Students should use the unlined side of standard *engineering paper* to neatly record their homework solutions. Be sure that you write your name and HW assignment number neatly at the top of each page; multiple pages should be stapled together (no paper clips or cute little folds—this isn't grade school). *Hint:* engineering problems are usually best solved using some variation of the "Given, Required, Solution, Answer" format. Be sure to write clearly and neatly, show all of your solution process, and clearly indicate your final answers by underlining them or drawing a box around them (or simply annotating if appropriate). The Student Grader is *not* required to decipher inscrutable handwriting; you could end up with a zero if your homework is difficult to read.

Late turn-ins will not be accepted unless an extraordinary situation exists. Very few circumstances constitute an extraordinary situation—so plan ahead! You can always drop off your assignment at your instructor's office before the due date. ☺

4.3 Grading Scale

The University of Wyoming recently implemented a grading policy that allows, at the instructor's discretion, use of a "plus, minus" grading system.[1] Since this is a relatively new option, your instructor wishes to give the students in the class the choice, in the form of a vote sent to me via email the first week of class, of whether of not to use the $+/-$ grading system. The thresholds and effect on GPA are provided in the following two tables for you to compare. The course will be graded on the selected scale, where the student's overall average in the course, as a percentage, is represented by x.

[1] See UW Regulation 6-722 for complete details. Note that the optional plus/minus grading system was voted on and approved by the UW Faculty Senate, approved by the UW Board of Trustees, and went into effect starting with the Fall 2014 semester. Whether or not it's used is left up to each instructor.

Grade	Course Average (%)	Equivalent GPA (4.00 scale)
A	$90 \leq x \leq 100$	4.00
B	$80 \leq x < 90$	3.00
C	$70 \leq x < 80$	2.00
D	$60 \leq x < 70$	1.00
F	$0 \leq x < 60$	0.00

Grade	Course Average (%)	Equivalent GPA (4.00 scale)
A	$93 \leq x \leq 100$	4.00
A−	$90 \leq x < 93$	3.67
B+	$86 \leq x < 90$	3.33
B	$83 \leq x < 86$	3.00
B−	$80 \leq x < 83$	2.67
C+	$76 \leq x < 80$	2.33
C	$73 \leq x < 76$	2.00
C−	$70 \leq x < 73$	1.67
D+	$66 \leq x < 70$	1.33
D	$60 \leq x < 66$	1.00
F	$0 \leq x < 60$	0.00

No grade curves or other adjustments to the scale should be expected.

5 Course Materials and Resources

5.1 Textbook

Our textbook, by Harris and Harris, is listed as [1] in the References section of this syllabus. This book provides good coverage of the topics, and emphasizes modern design methods. In this course, we will cover nearly the first half of the book (most of Chap. 1–5), with supplementary notes supplied as needed for certain topics (The second half of this book may be used for EE 4390). Take advantage of the many examples in the book, along with the very helpful end-of-chapter exercises and Interview Questions.[2]

5.2 eBooks

While the price of the textbook is extremely reasonable compared to most engineering texts, if you are a fan of electronic books (eBooks) you can access the textbook for free, as well as many other related textbooks and references. A very rich collection of textbooks in electronic form can be accessed through the University of Wyoming Library online eBook facility. If you'd like to investigate these resources, here's how simple it is:

[2]The Interview Questions are taken from a collection of actual questions that have been recently asked of job candidates applying for work in various fields closely related to Digital Design. Don't skip over these!

1. Open a web browser on your computer (FireFox, Chrome, etc.).
2. Point your browser at the following URL: `http://www-lib.uwyo.edu/`
3. Select the `eJournals & eBooks` link in the research tools banner on the lower middle of the page.
4. On the resulting search page(s), be sure to select the button under the "eBooks" category.
5. Use the "Title contains all words" method, and type or paste in the title, to search for any of the texts listed in this syllabus.
6. **Note:** If you are accessing the web search from a University wired or wireless connection, your searches and access to the eBooks should be transparent. If, however, you are accessing the web from off-campus, you will be asked to enter your account and password (UWYO domain information) when you first attempt to access an eBook.

While your textbook is freely available as an eBook,[3] there are many additional eBooks you may find helpful on the UW Library website. For example, the textbooks listed in the References section of this syllabus as [2, 3, 4, 5] provide reasonable discussions of the majority of the fundamentals of digital system design. The texts listed as [6, 7, 8] are excellent references for the use of the Verilog HDL (hardware description language). Regarding Verilog books, be careful about the publication date and which version of Verilog is covered in the book. Verilog and SystemVerilog merged in 2009, but many books have not caught up to that change (your textbook has, but the Xilinx ISE tools have not).

Additional references pertinent to this course are also listed in the References section of this syllabus; they may or may not be available as eBooks.

5.3 Lecture Slides

Extensive lecture slides will be used throughout the course that will cover all the topics discussed in class. Copies of these slides will be available on the course website in PowerPoint file format.

5.4 For More Practice

If you learn best using extensive problem sets and worked examples, it's difficult to find anything better than the Schaum's Outline Series. **These titles are not available in free eBook form from the Library facility; however, they are quite inexpensive in print form from distributors such as Amazon or Barnes & Noble.** For this course, the texts listed as [9, 10, 11] provide a large number of problems and solutions. Don't worry about the "old" publication dates; the underlying principles covered in these books haven't changed!

[3] Careful: both the second edition and the first edition will be listed as eBooks. You will almost certainly want the second edition, except perhaps for Chapter 4 to see Verilog code rather than SystemVerilog code.

5.5 Web Site

For this course, we will make frequent use of the course website located at

`https://uwyo.instructure.com/courses/327258`

Note: This site is hosted under the WyoCourses system. It is a secure web host for UW students, and you will need to log in with your normal UW student account details. **We will mainly use the Files area of the website.** A copy of this syllabus, lecture slides, assignments, detailed homework solutions, some lecture notes, Verilog examples, and other supplemental material will be posted on this web site, organized into subdirectories with self-explanatory names. You are responsible for checking this website regularly.

Another web site you may find quite helpful and useful is the textbook companion website maintained by the publisher. You can use the URL listed in the book's Preface (see p. xxi) or the more direct URL given below.

`http://booksite.elsevier.com/9780123944245/`

This is a richly populated web site with solutions to odd-numbered problems, all the figures in the book, example lecture slides, tutorials, links to helpful other sites, etc. You are encouraged to take advantage of it!

5.6 Software and Other Resources

All software described here is freely available online. To complete the lab exercises, each student must become familiar with a professional-grade software package for digital design. The primary software used in the lab is:

- **Xilinx ISE WebPACK (14.1 or newer, current version is 14.7).** This software is already installed on ECE Dept computers (ECE Digital Lab, EN 5030 and ECE Computer Lab, EN 5038). If you wish your own copy (the WebPACK is free), the download is rather large, and you'll encounter several installation questions (e.g., product registration and license manager installation) if you choose to proceed. The process begins at `http://www.xilinx.com/`. Be sure to download ISE, not Vivado. The Vivado Design Tools do not support the board you will purchase for use in lab.

For practicing basic digital design with common logic gates and verifying the design via simulation, a very nice, simple simulator is:

- **Logisim.** This free program is a Java-based (therefore platform independent) visual simulator for simple digital circuits. See the instructions for download at `http://www.cburch.com/logisim/index.html`. A Windows executable file of this simulator is also available on the ECE network drive described in the EE 2390 Lab manual.

Needed to solve some homework problems and also for practice using Verilog to create and test various digital designs using something smaller and simpler than the Xilinx ISE program, a very nice software tool is:

- **Icarus Verilog and GTKWave:** These free programs provide a lightweight, clean and simple *command-line* Verilog compiler and waveform viewer. Available for Windows, Linux and Mac OS X. Use a Google search for your preferred platform download. A Windows compatible install file for these two tools is also available on the ECE network drive described in the EE 2390 Lab manual, in the `iverilog` directory.

Important Note: Most of the lab exercises will require the use of an inexpensive student-owned Basys2 board manufactured by Digilent, Inc. See `http://www.digilentinc.com/Products/Detail.cfm?Prod=BASYS2&NavT` for details. The Basys2 board is a circuit design and implementation platform for digital circuits. Built around a Xilinx Spartan-3E Field Programmable Gate Array (FPGA), the Basys2 board provides a complete, ready-to-use hardware (and firmware) platform suitable for implementing a wide variety of digital designs. A large collection of on-board I/O devices and all required FPGA support circuits are included on the board, and it easily connects to your computer via a USB port. **Each student must purchase their own Basys2 board in time to have it in hand in time for Lab 4.** The academic price of this board as of this writing is $69; you may also find you can use it for other classes and perhaps for your Senior Design project.

6 Miscellaneous Course Policies

6.1 Collaboration Policy

To solve the homework assignments and Prelabs, you are encouraged to work with other students currently enrolled in EE 2390. Don't try to use, and most certainly don't copy, homework or lab exercise solutions from previous semesters. Not only is it academically dishonest to do so, but a very subtle change in the assignment can cause significant changes in the correct solution. It is very obvious when a student turns in a solution to a previous semester's assignment.

For allowed collaborations, you must document *any* of the help you receive in the form of comments directly on your homework paper or in your lab notebook as appropriate. No comments mean you are submitting the item as *totally* your own work; my assumption will always be that you are an honorable person unless you cause me to believe otherwise. Simply copying another person's assignment is, of course, not allowed—the actual item you turn in must ultimately be your own work. You may be called to your instructor's office with no advance notice to explain in detail the specifics of your work.

Quizzes and exams must always be the *student's own work*.

6.2 Academic Honesty

"The University of Wyoming is built upon a strong foundation of integrity, respect and trust. All members of the University community have a responsibility to be honest and have the right to expect honesty from others. Any form of academic dishonesty is unacceptable to our community and will not be tolerated." [excerpted from the UW General Bulletin] All persons should report suspected violations of standards of academic honesty to the instructor, department head, or dean. See UW Regulation 6-802, "Procedures and Autho-

rized University Actions in Cases of Student Academic Dishonesty." You can read this and all other University regulations at: `http://www.uwyo.edu/generalcounsel/index.html`

6.3 Disability Statement

If you have a physical, learning, or psychological disability and require accommodations, please let the instructor know as soon as possible. You must register with, and provide documentation of your disability, to University Disability Support Services (UDSS) in SEO, room 330 Knight Hall.

7 Laboratory

Important note: ***Attendance at labs is required.*** You must attend the lab section in which you are enrolled. Satisfactory completion of *each and every* lab exercise is *required* in order to pass the course. **This is strictly enforced!** That may sound harsh, but that's the deal. Refer to the EE 2390 Laboratory Policies handout for further details. *Note:* For scheduling purposes, **lab sections will not meet the first week of class.** The first lab meeting will be Tuesday, February 3, 2015.

8 Course Overview

Welcome to EE 2390! This course will prepare you to deal competently with myriad digital system design challenges that regularly confront electrical and computer engineers. The emphasis in EE 2390 is on fundamental principles and practical applications, rather than esoteric theory or arcane derivations.

Just like with anything worthwhile in life, if you aren't willing to put in the time and effort, you won't ever become good at it. Be prepared to devote considerable time and effort to this class. I promise to be sensitive to the time requirements of every assignment I give you, but *you* have to put forth the effort. As Robert E. Heinlein was known to say, "TANSTAFL." Do you know what that stands for?

Some recommendations for success in this class which you might want to consider...

Don't miss class. New material, some of which is not in the text, is covered each lecture. Attendance at lecture isn't required, but if you miss class, *you* are responsible for covering the missed material on your own.

Read in advance. The reading assignments are listed in the next section. Your textbook is quite readable, and you are *expected* to read it. Whining that "the book is too hard to read" receives very little respect in any forum.

Start homework early. Give yourself enough time to consider the problems and determine whether or not you need assistance of another student or your instructor. Last-minute questions are a bad idea, and you probably won't like the answer.

Don't "blow off" homework, labs, or quizzes. They comprise 35% of your grade!

Ask questions. This includes during class and during office hours. I don't like a silent class—feel free to ask questions or make reasonable comments at will (but no distracting side conversations, please).

Don't arrive late for class. If you know you'll be delayed (or absent) for some reason, just let me know ahead of time in person or via e-mail. It's the courteous and adult thing to do.

Let's have fun in this class! I like lively, attentive, alert students with an active sense of humor. It's more fun that way for all of us...

9 Course Schedule

This is an approximate lesson-by-lesson schedule, *subject to change*.

Week	Lecture Number	Date	Day of Week	Topic	Text Reading	HWK Due
1	1	26-Jan-2015	M	Intro to Digital Systems, Binary Number Systems, Hex, Octal	Ch. 1, pp. 3--14	
	2	28-Jan-2015	W	Number Complements, Arithmetic Addition and Subtraction	Ch. 1, pp. 14--19	
	3	30-Jan-2015	F	Binary Codes, BCD, Excess-3, Gray Code, ASCII, Parity	Notes	HW 1
2	4	2-Feb-2015	M	Logic Gates and Physical Implementations	Ch. 1, pp. 19--26	
	5	4-Feb-2015	W	Combinational Logic Terminology	Ch. 2, pp. 55--60	
	6	6-Feb-2015	F	Boolean Algebra Axioms and Theorems	Ch. 2, pp. 60--66	HW 2
3	7	9-Feb-2015	M	Digital Logic Gates, Schematics, Manipulations	Ch. 2, pp. 66--75	
	8	11-Feb-2015	W	Gate-Level Minimization, Karnaugh Maps	Ch. 2, pp. 75--81	
	9	13-Feb-2015	F	More Karnaugh Maps, Don't Cares, NAND-NAND / NOR-NOR	Ch. 2, pp. 81--83	HW 3
4	10	16-Feb-2015	M	Introduction to HDLs	Ch. 4, pp. 173--186	
	11	18-Feb-2015	W	Combinational Logic Building Blocks (mux, decoders)	Ch. 2, pp. 83--88	
	12	20-Feb-2015	F	Timing, Delay, and Glitches	Ch. 2, pp. 88--95	HW 4
5	13	23-Feb-2015	M	More Verilog HDL for Combinational Logic	Ch. 4, pp. 186--193	
	14	25-Feb-2015	W	More HDL, Test Benches	Ch. 4, pp. 220--224	
	15	27-Feb-2015	F	Summary for Exam #1		HW 5
6	16	2-Mar-2015	M	**Exam #1**		
	17	4-Mar-2015	W	Intro to Synchronous Sequential Logic Systems	Ch. 3, pp. 109--113	
	18	6-Mar-2015	F	Flip-Flop Storage Elements (D, plus JK and T, from notes)	Ch. 3, pp. 114-118	
7	19	9-Mar-2015	M	Synchronous Logic Design	Ch. 3, pp. 119--123	
	20	11-Mar-2015	W	State Reduction and Assignment, Excitation Tables	Notes	
	21	13-Mar-2015	F	Design and Analysis of Synchronous State Machines	Ch. 3, pp. 123--141	HW 6
8	No class	16-Mar-2015	M	**Spring Break, no classes**		
	No class	18-Mar-2015	W	**Spring Break, no classes**		
	No class	20-Mar-2015	F	**Spring Break, no classes**		
9	22	23-Mar-2015	M	Sequential Logic Description with Verilog HDL	Ch. 4, pp. 193--209	
	23	25-Mar-2015	W	More Finite State Machine Synthesis with Verilog HDL	Ch. 4, pp. 209--213	
	24	27-Mar-2015	F	Registers	Notes	HW 7
10	25	30-Mar-2015	M	Counters	Ch. 5, pp. 261--263	
	26	1-Apr-2015	W	More about Registers and Counters	Ch. 5, pp. 260--261	
	27	3-Apr-2015	F	Verilog HDL for Registers and Counters	Notes	HW 8
11	28	6-Apr-2015	M	Introduction to Register Transfer Level (RTL) Methods	Notes	
	29	8-Apr-2015	W	ASM Design Example	Notes	
	30	10-Apr-2015	F	ASM Description in Verilog HDL	Notes	HW 9
12	31	13-Apr-2015	M	Complex ASM Design in Verilog HDL	Notes	
	32	15-Apr-2015	W	Advanced ASM Design Techniques	Notes	
	33	17-Apr-2015	F	Summary for Exam #2		HW 10
13	34	20-Apr-2015	M	**Exam #2**		
	35	22-Apr-2015	W	Advanced Arithmetic Circuits	Ch. 5, pp. 239--254	
	36	24-Apr-2015	F	Advanced Number Systems: fixed and floating point	Ch. 5, pp. 255--259	
14	37	27-Apr-2015	M	Advanced Number Systems: fixed and floating point (continued)		
	38	29-Apr-2015	W	Memory, Verilog HDL Description (plus addressing, from notes)	Ch. 5, pp. 263--272	
	39	1-May-2015	F	Error Detection and Correction Examples, ROM	Notes	HW 11
15	40	4-May-2015	M	PLAs, PLDs, CPLDs and FPGAs	Ch. 5, pp. 272--280	
	41	6-May-2015	W	Advanced Digital Design Example	Notes	
	42	8-May-2015	F	Summary for Final Exam		HW 12
		15-May-2015	F	**Final Exam time: 10:15 AM to 12:15 PM**		

References

[1] D. M. Harris and S. L. Harris, *Digital Design and Computer Architecture*, Morgan Kaufmann Publishers, 2nd ed., 2013. ANNOTATION: An excellent, succinct text that emphasizes the latest design methods and Verilog coding styles.

[2] B. Holdsworth and C. Woods, *Digital Logic Design*, Newnes Publishing, 4th ed., 2002.

[3] C. Maxfield, *Bebop to the Boolean Boogie: An Unconventional Guide to Electronics*, Newnes Publishing, 3rd ed., 2009. ANNOTATION: A truly great book! This book is fun to read; you can learn all about digital logic while being entertained by this talented author. Too bad it isn't quite suitable as a textbook, but you do get a good seafood gumbo recipe in the appendix!

[4] C. Maxfield, *The Design Warrior's Guide to FPGAs: Devices, Tools and Flows*, Newnes Publishing, 2004. ANNOTATION: Another great book by "Max" Maxfield! While more advanced than his "Boogie" book, this book is similarly fun to read; you can learn all about state-of-the-art programmable digital logic without getting bored. It's a quick and informative read.

[5] R. Kamal, *Digital Systems Principles and Design*. Pearson Education India, 2006.

[6] R. B. Reese and M. A. Thornton, *Introduction to Logic Synthesis using Verilog HDL*. Morgan & Claypool Publishers, 2006. ANNOTATION: A very good book by co-writtem by a friend of your professor. Note that a very large collection of Morgan & Claypool technical books are available to UW students free of charge.

[7] S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*. Prentice Hall PTR, 2nd ed., 2003. ANNOTATION: One of my favorite introductory Verilog books. A bit harder to read than Bhasker's book, but very complete and well organized.

[8] P. J. Ashenden, *Digital Design: An Embedded Systems Approach Using Verilog*, Morgan Kaufmann Publishers, 2008.

[9] J. Palmer and D. Perlman, *Schaum's Outline of Theory and Problems of Introduction to Digital Systems*, McGraw-Hill, 1993.

[10] R. L. Tokheim, *Schaum's Outline of Theory and Problems of Digital Principles*, McGraw Hill, 1994.

[11] E. Mendelson, *Schaum's Outline of Theory and Problems of Boolean Algebra and Switching Circuits*, McGraw Hill, 1970.

[12] M. M. Mano and M. D. Ciletti, *Digital Design*. Prentice Hall, 5th ed., 2012. ANNOTATION: A very complete yet readable introductory text. Many excellent digital logic examples, but uses a dated treatment of Verilog HDL.

[13] J. F. Wakerly, *Digital Design: Principles and Practices*. Prentice Hall, 4th ed., 2006. ANNOTATION: A densely written but extremely informative book on digital design. Considered by many to be one of the definitive texts on the subject, it is sometimes

used for introductory courses but also is used in more advanced courses. An excellent reference book for your professional library.

[14] J. Bhasker, *A Verilog HDL Primer*. Star Galaxy Publishing, 3rd ed., 2005. ANNOTATION: A very easy to read introduction to Verilog, but a bit on the elementary side. Based on the older Verilog 2001 Standard, and does not cover SystemVerilog.

[15] K. Coffman, *Real World FPGA Design with Verilog*. Prentice Hall PTR, 2000. ANNOTATION: A bit advanced, but as the title says it is full of real-world practical tips. Uses an older form of Verilog, but still useful.

[16] M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*. Pearson/Prentice Hall, 2nd ed., 2010. ANNOTATION: An advanced but fairly well written text with lots of examples. Unfortunately, uses a dated treatment of Verilog

[17] M. D. Ercegovac and T. Lang, *Digital Arithmetic*. Morgan Kaufmann Publishers, 2004. ANNOTATION: A detailed treatment of all types of computer-based mathematics, number systems, and numerical representations.

Only one more page to go...

Finally...

Congratulations on reading this far! Lesser mortals gave up a page or two ago. As a reward, perhaps these quotes will inspire you in a positive manner...

Any fool can know. The point is to understand.
—Albert Einstein

The beginning of knowledge is the discovery of something we do not understand.
—Frank Herbert

To study, and when the occasion arises to put what one has learned into practice—is that not deeply satisfying?
—Confucius

The trouble with quotes from the Internet is you can never tell if they're genuine...
—Abraham Lincoln

They never said it would be easy, but they never said it'd be this hard.
They never said it would be easy, but I never thought we'd come this far.
—Sheryl Crow

That which does not kill us makes us stronger.
—Friedrich Nietzsche